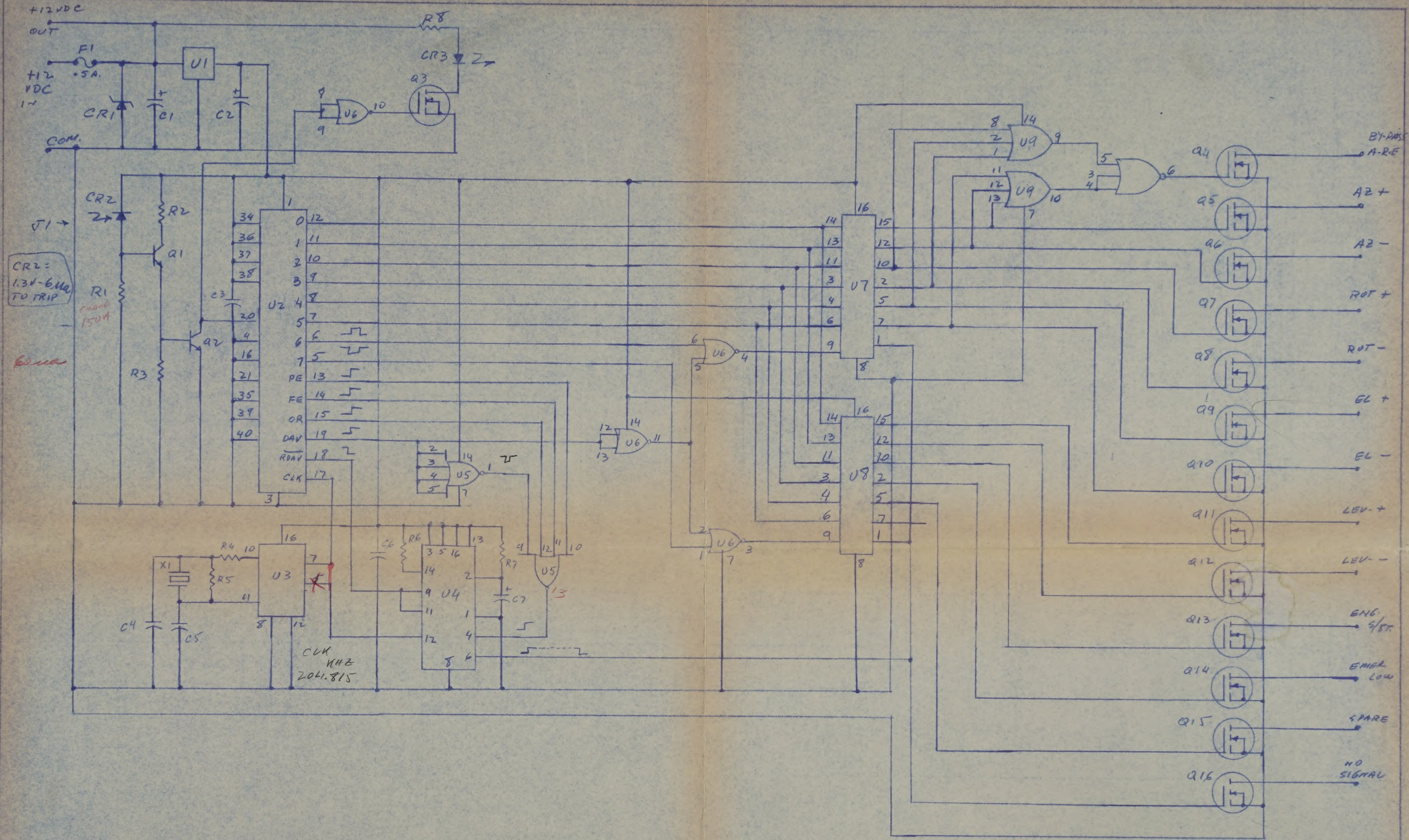

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3. PARTS LIST: PL101847
2. ASSEMBLY: 101849
1. TOP DRAWING: 101847
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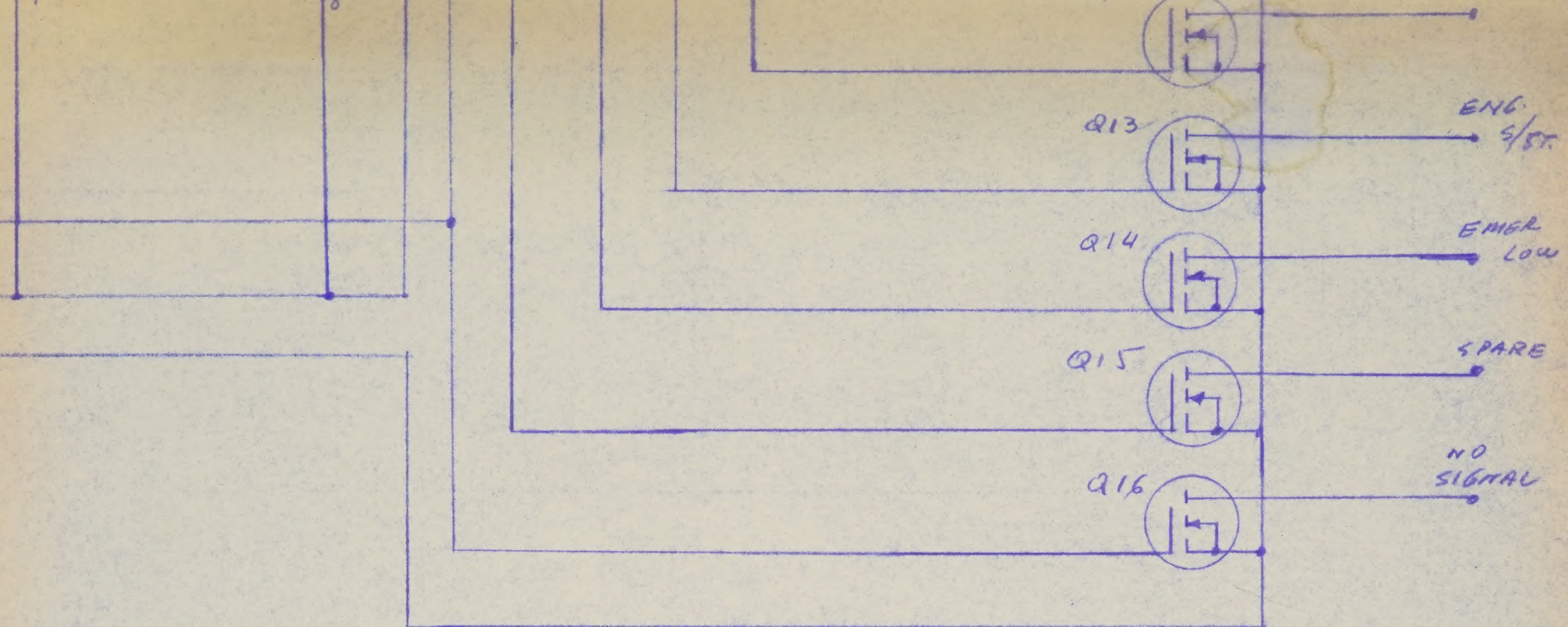
DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR [signature] 3-16-89	**Parko** ELECTRONICS COMPANY INC., SANTA ANA, CALIF.	
TOLERANCES (unless otherwise specified) .X ±.1 .XX ±.03 .XXX±.010 ANGLES±0.5°	CHK	OPTICAL LINK RECEIVER	
	DSGN		
	PROJ		
	REL		
MACH SURF √	APPROVED	CODE IDENT NO. 13979	SIZE 101848 REV
	APPROVED		
	DO NOT SCALE DRAWING	SCALE	SHEET OF



DIMENSIONS ARE IN INCHES AND AFTER PLATING

TOLERANCES (unless otherwise specified)
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.XX ±.03
.XXX±.010
ANGLES±0.5°
MACH SURF √

DR [illegible]	3-16-89
CHK	
DSGN	
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REL	

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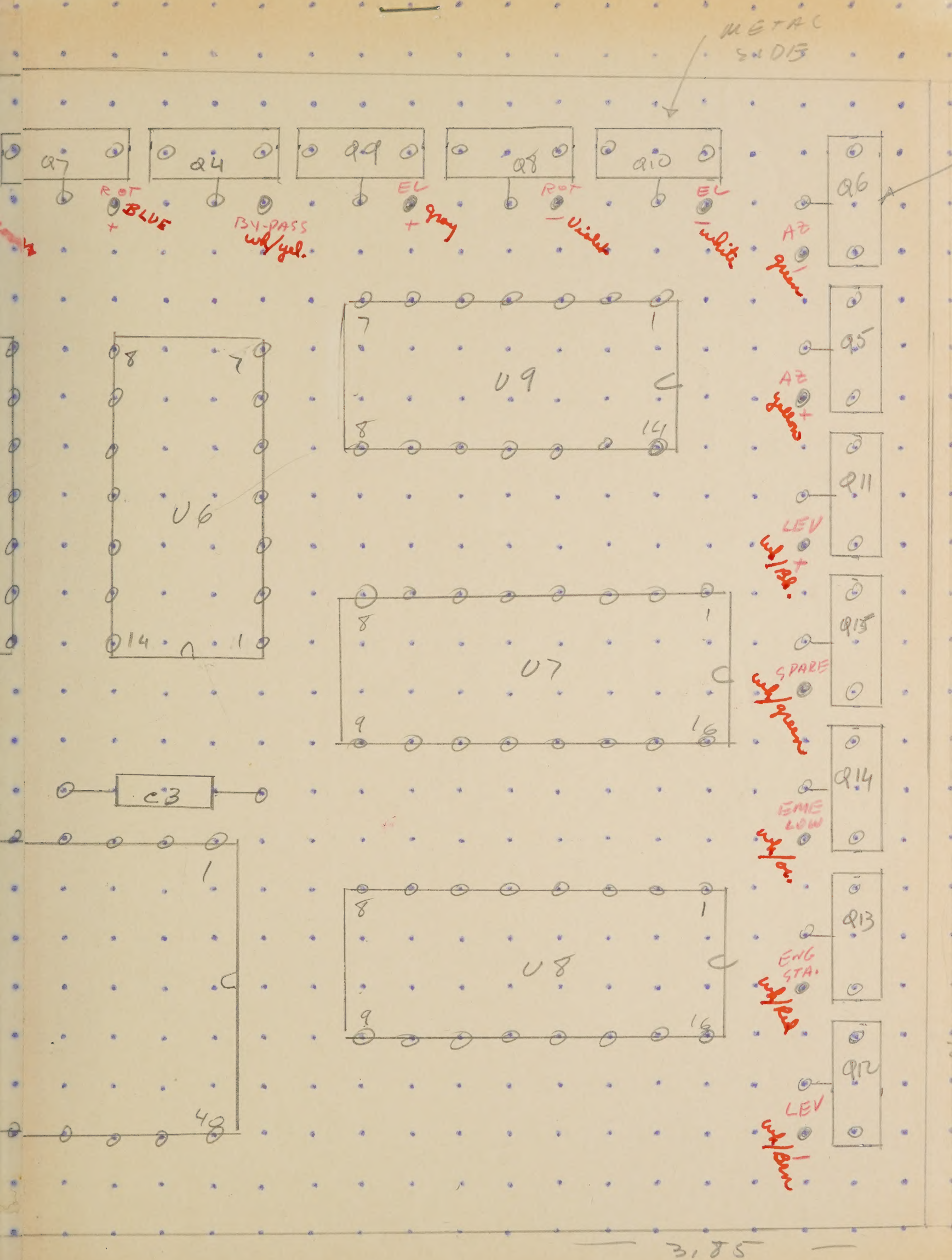
APPROVED

DO NOT SCALE DRAWING

Parko
ELECTRONICS COMPANY INC., SANTA ANA, CALIF.

OPTICAL LINK RECEIVER

CODE IDENT NO.	SIZE		REV
13979		101848	
SCALE		SHEET OF	



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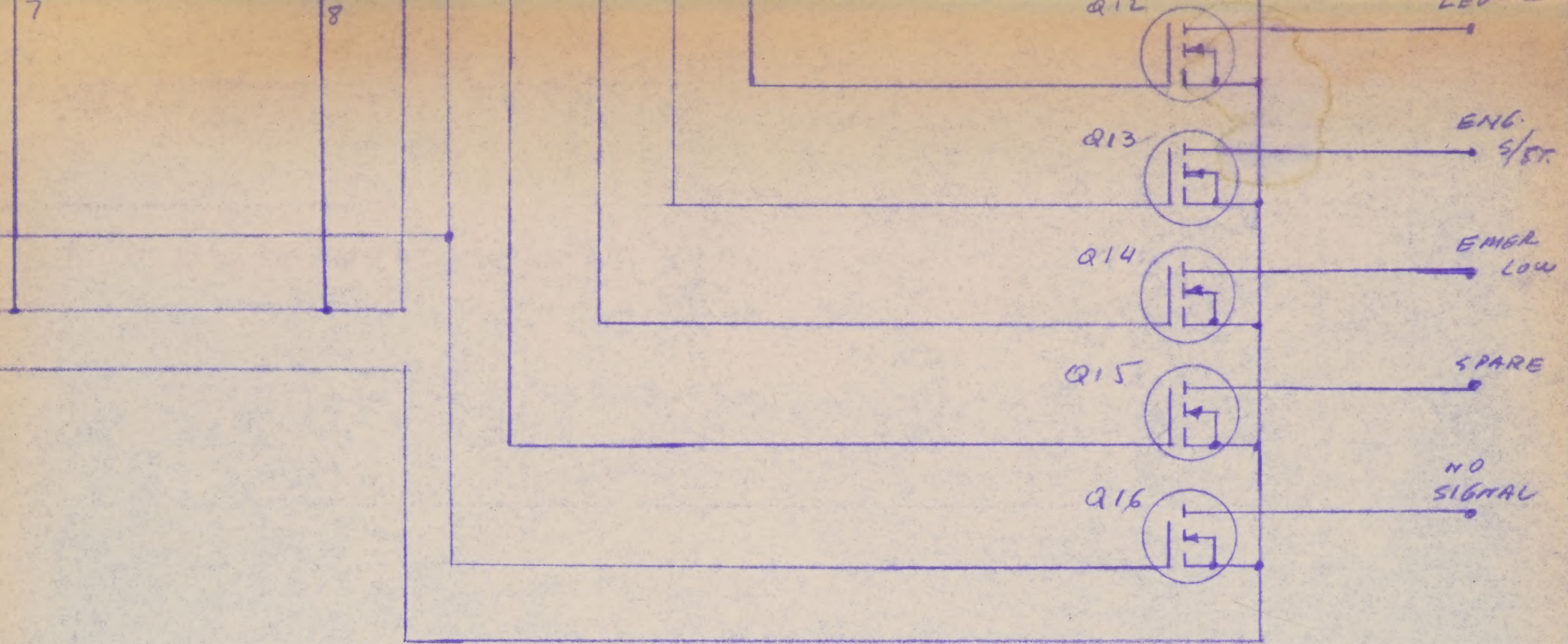
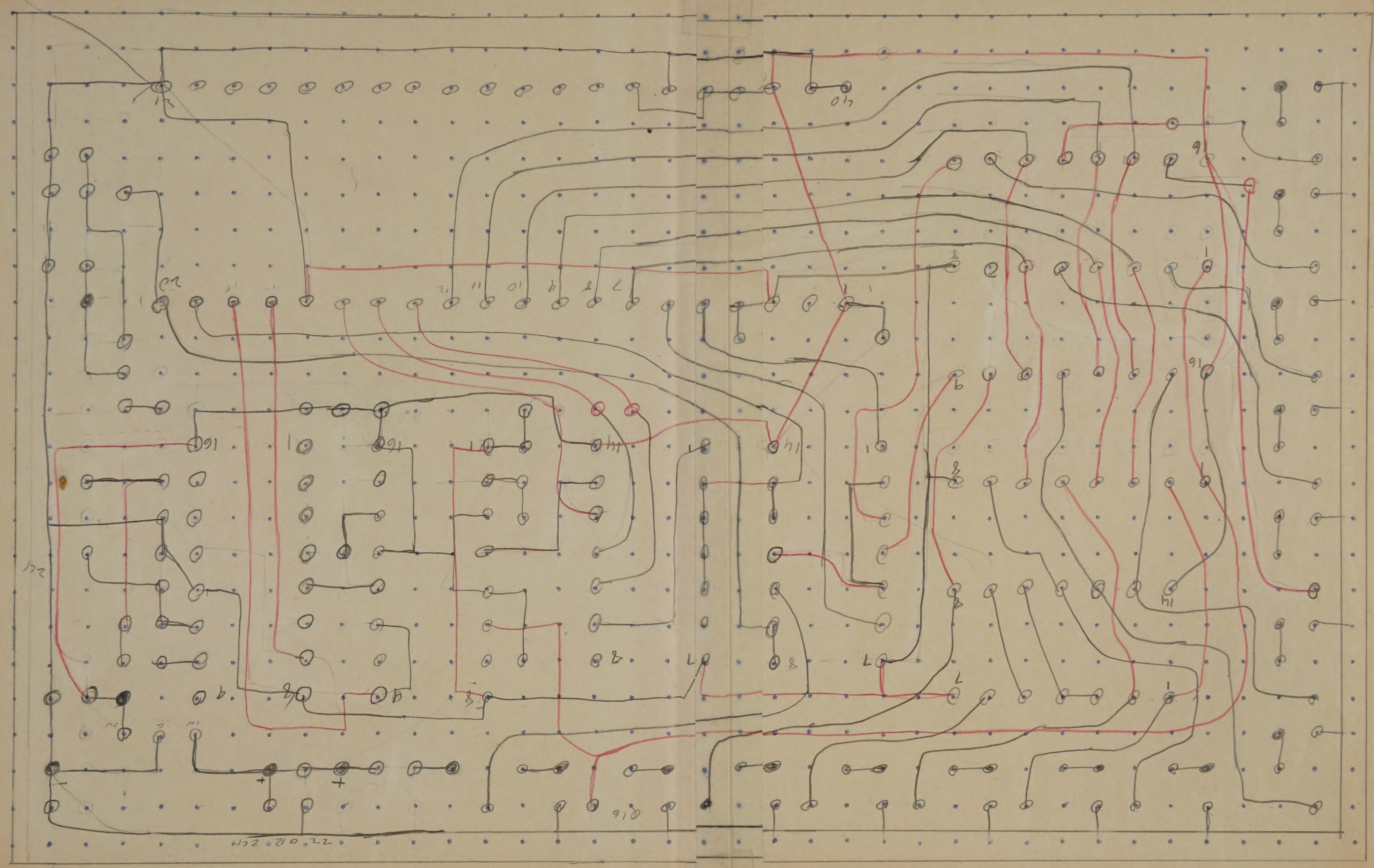
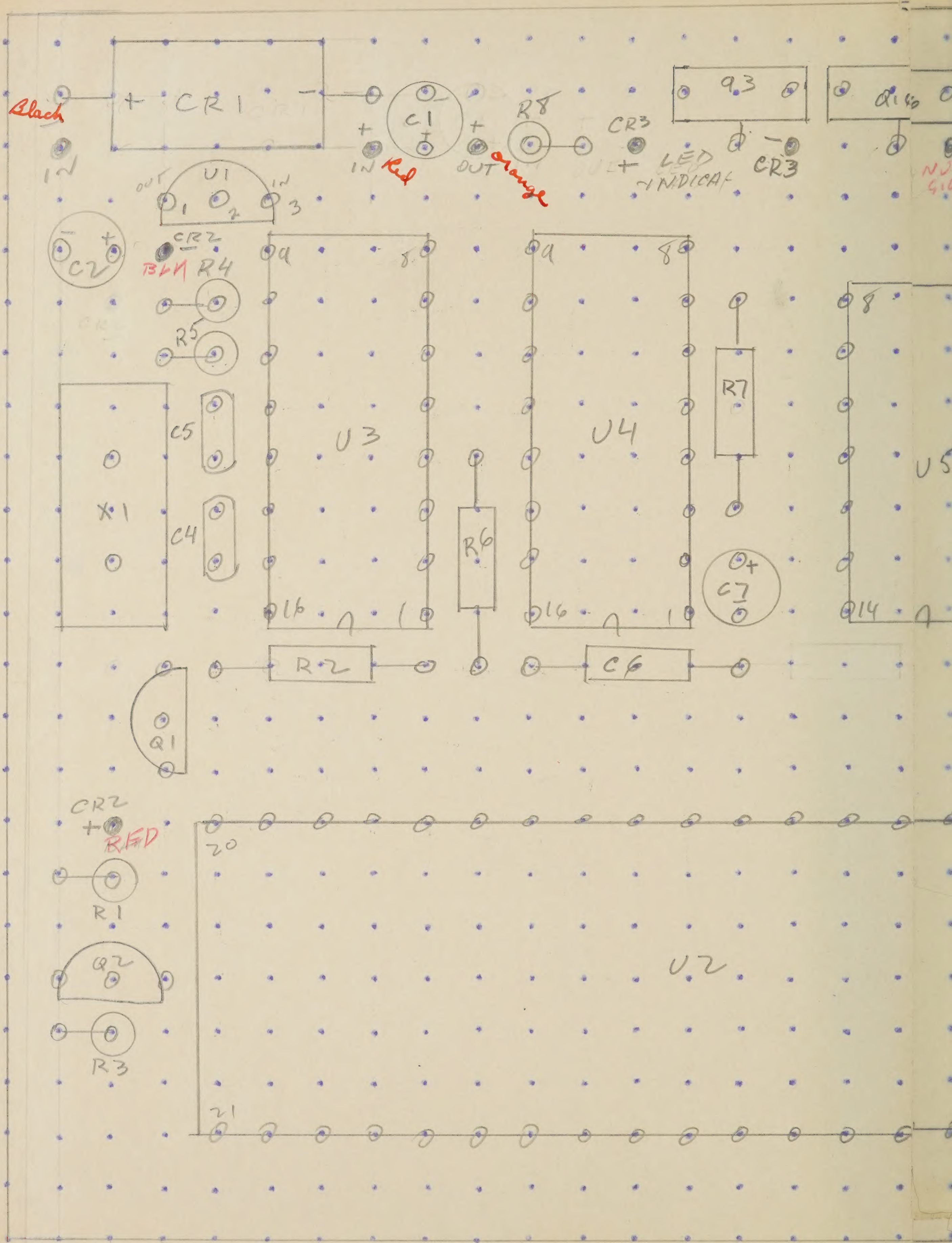


DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR [signature]	3-16-89	**Parko** ELECTRONICS COMPANY INC., SANTA ANA, CALIF.	
TOLERANCES (unless otherwise specified) .X ±.1 .XX ±.03 .XXX±.010 ANGLES±0.5° MACH SURF ✓	CHK		OPTICAL LINK RECEIVER	
	DSGN			
	PROJ			
	REL			
	APPROVED		CODE IDENT NO. 13979	SIZE 101848 REV
	APPROVED			
	DO NOT SCALE DRAWING		SCALE	SHEET OF




Black
CR1
IN
C1
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Red
R8
OUT
Orange
CR3
LED
INDICAT
Q3
CR3
U1
OUT
IN
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2
3
C2
CR2
BLK
R4
R5
C5
C4
X1
9
8
U3
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9
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U4
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R6
R7
C7
8
U5
14
R2
C6
Q1
CR2
RED
R1
Q2
R3
20
U2
21

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Designer's Data Sheet

TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

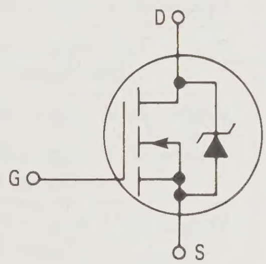
MTD3055EL

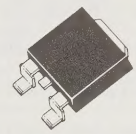
TMOS POWER MOSFET
LOGIC LEVEL
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
60 VOLTS

This advanced E-FET is a TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

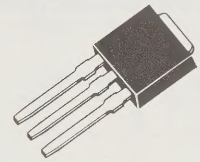
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at 150°C
- Available With Long Leads, Add -1 Suffix

TMOS





CASE 369A-04
MTD3055EL



CASE 369-03
MTD3055EL-1

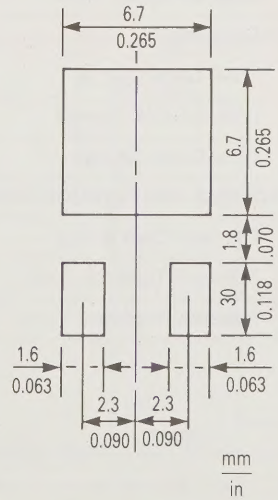
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

MINIMUM PAD SIZES
RECOMMENDED FOR
SURFACE MOUNTED
APPLICATIONS



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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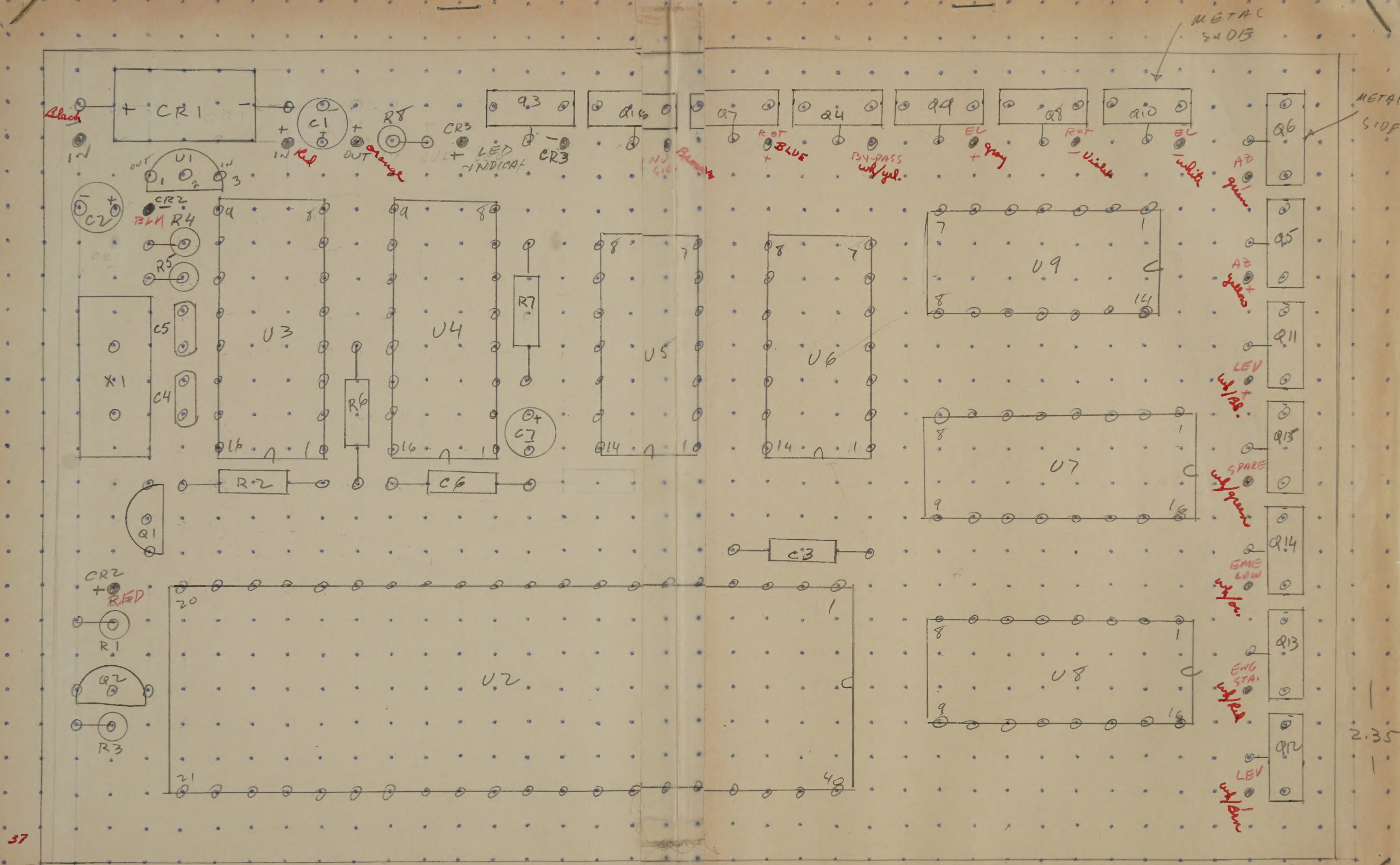
MOTOROLA



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MTD3055EL

Designer's Data Sheet

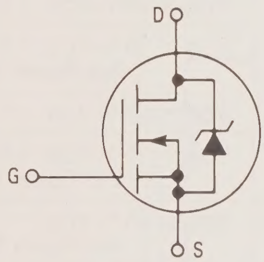
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

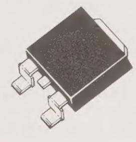
**TMOS POWER MOSFET
LOGIC LEVEL
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
60 VOLTS**

This advanced E-FET is a TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

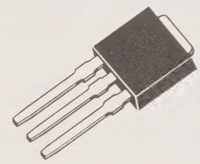
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at 150°C
- Available With Long Leads, Add -1 Suffix

TMOS™





CASE 369A-04
MTD3055EL



CASE 369-03
MTD3055EL-1

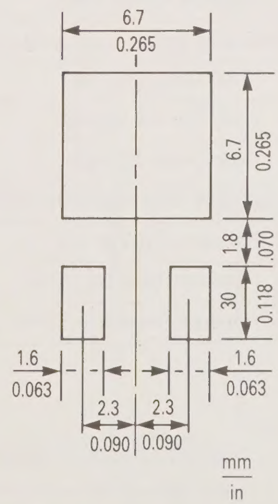
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

TMOS is a trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = 60 V, V_{GS} = 0)			—	1	
(V_{DS} = 60 V, V_{GS} = 0, T_J = 150°C)			—	50	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)			1	2	
T_J = 150°C			0.6	1.6	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V)		$V_{DS(on)}$			Vdc
(I_D = 12 Adc)			—	2.4	
(I_D = 6 Adc, T_J = 150°C)			—	1.95	
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14		W_{DSR}			mJ
(I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive)			—	18	
(I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)			—	35	
(I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)			—	16	
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	400 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		1000 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	30 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		660 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 15	C_{oss}	175 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time		t_r	95 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	38 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	11 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time	(I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	55 (Typ)	—	ns

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operatión for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

Figure 11. Commutating Safe Operating Area (CSOA)

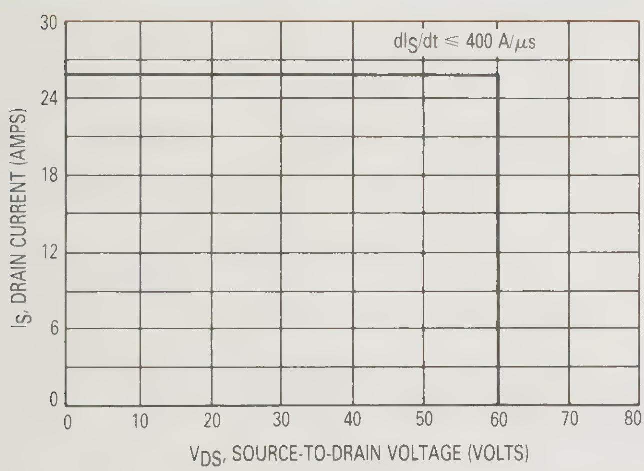


Figure 13. Unclamped Inductive Switching Test Circuit

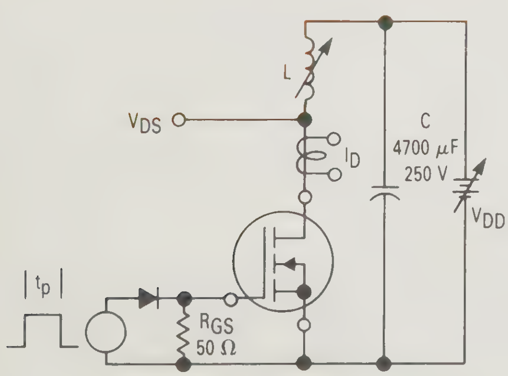


Figure 10. Commutating Waveforms

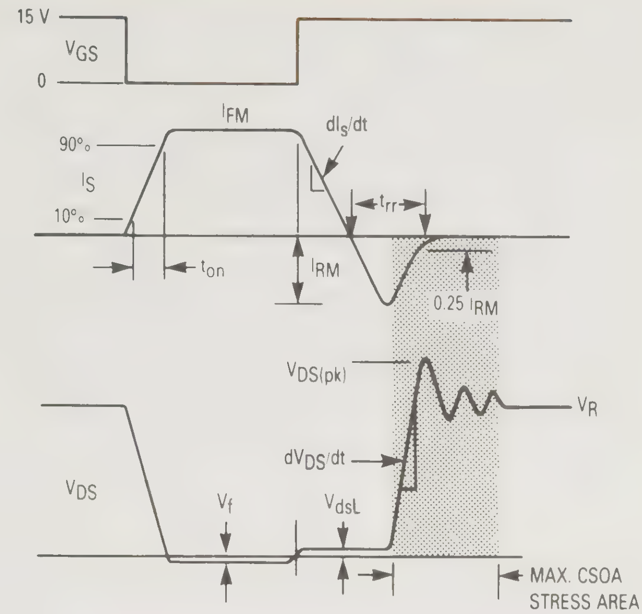


Figure 12. Commutating Safe Operating Area Test Circuit

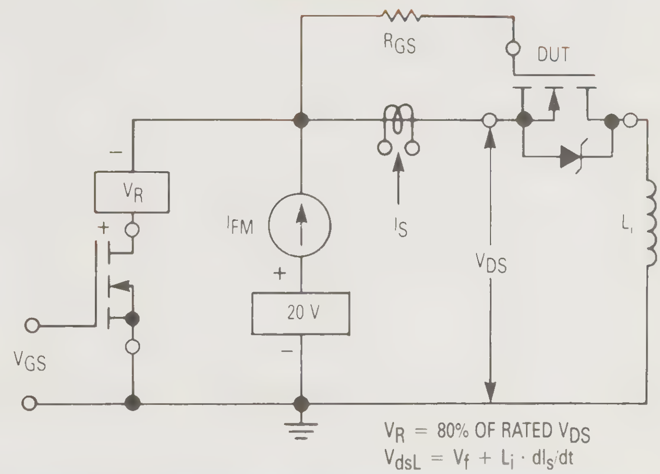
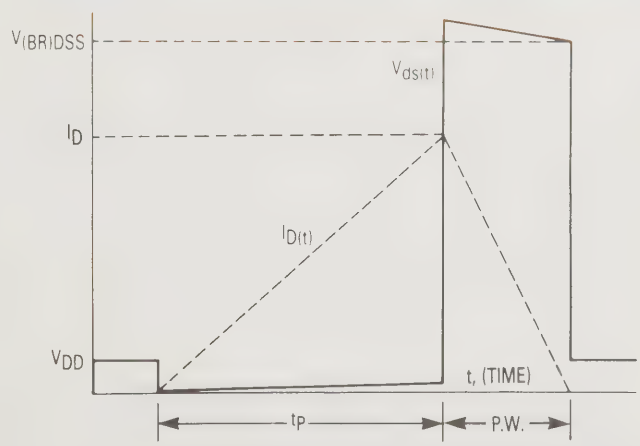


Figure 14. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0) (V_{DS} = 60 V, V_{GS} = 0, T_J = 150°C)	I_{DSS}	 — —	 1 50	µA
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 150°C	$V_{GS(th)}$	 1 0.6	 2 1.6	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 150°C)	$V_{DS(on)}$	 — —	 2.4 1.95	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14 (I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 100 µs, Duty Cycle ≤ 1%) (I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 µs, Duty Cycle ≤ 1%)	W_{DSR}	 — — —	 18 35 16	mJ

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	400 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		1000 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	30 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		660 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 15	C_{oss}	175 (Typ)	—	pF

SWITCHING CHARACTERISTICS (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time		t_r	95 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	38 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	11 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time	(I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/µs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	55 (Typ)	—	ns

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0) (V_{DS} = 60 V, V_{GS} = 0, T_J = 150°C)	I_{DSS}	— —	1 50	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 150°C	$V_{GS(th)}$	1 0.6	2 1.6	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 150°C)	$V_{DS(on)}$	— —	2.4 1.95	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14 (I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%) (I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)	W_{DSR}	— — —	18 35 16	mJ
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	400 (Typ)	—	pF
Input Capacitance (V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz, See Figure 15)	C_{iss}	1000 (Typ)	—	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	30 (Typ)	—	pF
Reverse Transfer Capacitance (V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz, See Figure 15)	C_{rss}	660 (Typ)	—	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 15)	C_{oss}	175 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time	t_r	95 (Typ)	—	
Turn-Off Delay Time	$t_{d(off)}$	38 (Typ)	—	
Fall Time	t_f	50 (Typ)	—	
Total Gate Charge (V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	11 (Typ)	17	nC
Gate-Source Charge	Q_{gs}	4 (Typ)	—	
Gate-Drain Charge	Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS				
Forward On-Voltage (I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time (I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	55 (Typ)	—	ns

TYPICAL ELECTRICAL CHARACTERISTICS

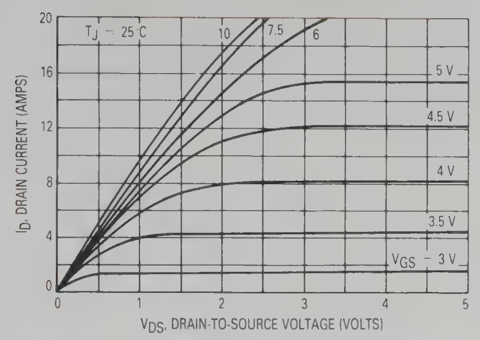


Figure 1. On-Region Characteristics

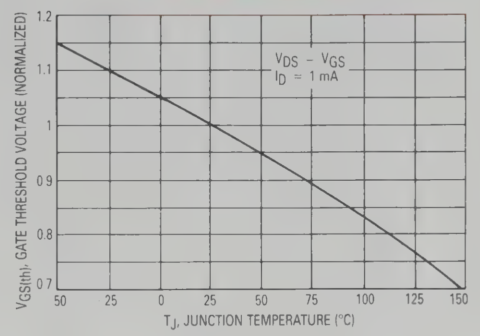


Figure 2. Gate-Threshold Voltage Variation With Temperature

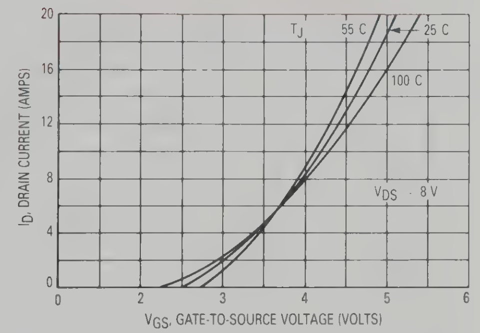


Figure 3. Transfer Characteristics

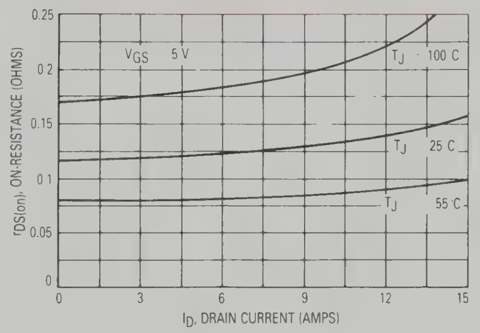


Figure 4. On-Resistance versus Drain Current

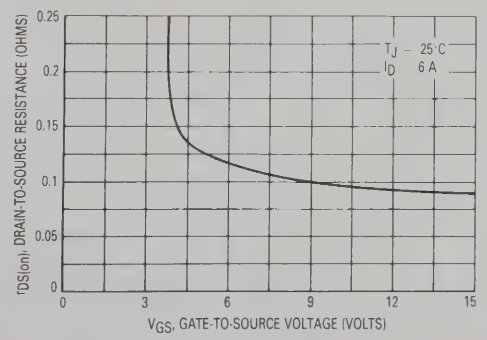


Figure 5. On-Resistance versus Gate-to-Source Voltage

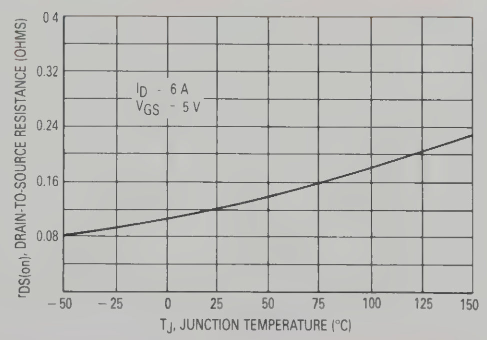


Figure 6. On-Resistance Variation With Temperature

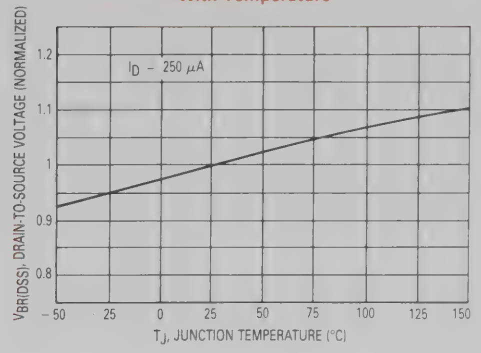


Figure 7. Breakdown Voltage Variation With Temperature

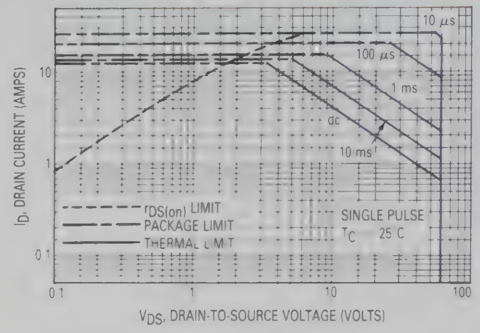


Figure 8. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response

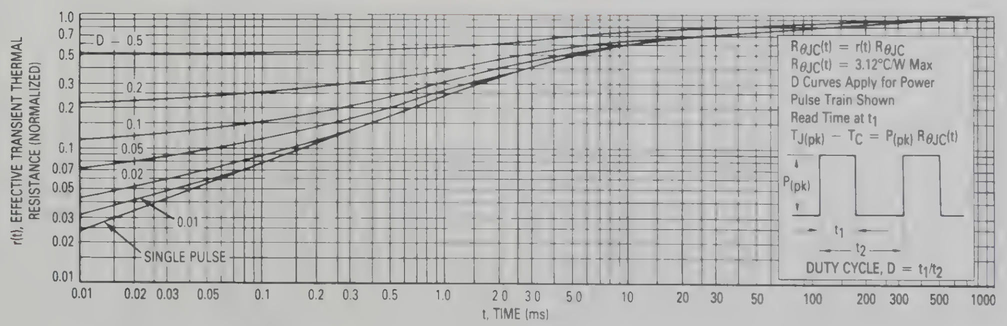


Figure 15. Capacitance Variation

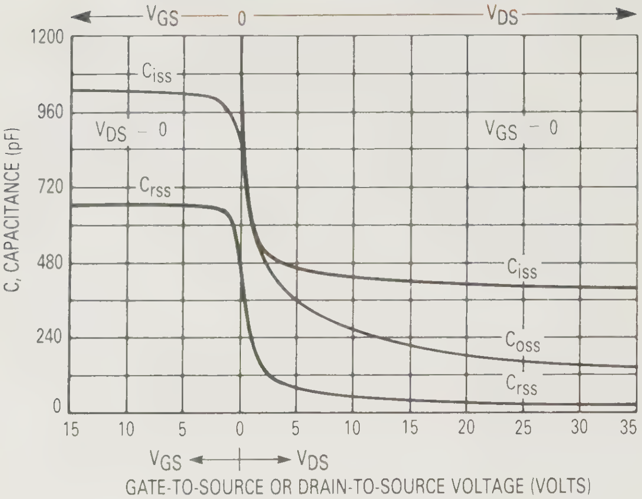


Figure 16. Gate Charge versus Gate-to-Source Voltage

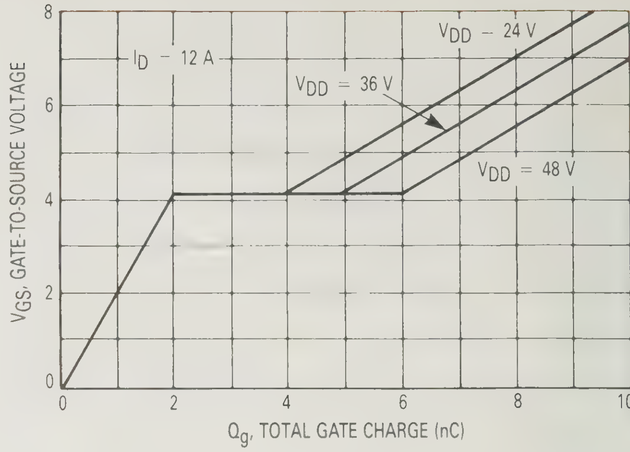
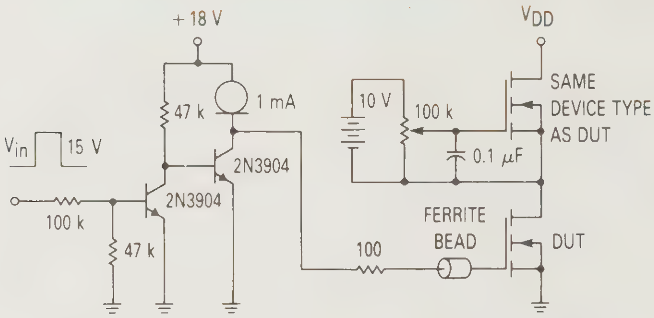
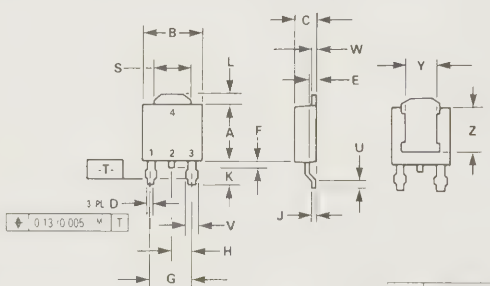


Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS

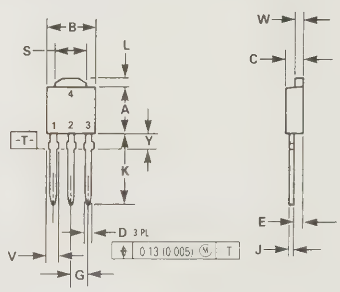


STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 SURFACE "T" IS BOTH A DATUM AND A SEATING PLANE
2 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
3 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5 97	6 22	0.235	0 245
B	6 35	6 73	0 250	0.265
C	2 19	2 38	0.086	0.094
D	0 69	0 88	0.027	0.035
E	0 97	1 06	0.038	0.042
F	0 64	0 88	0.025	0.035
G	4 58 BSC		0.180 BSC	
H	2 29 BSC		0 090 BSC	
J	6 46	0 58	0.018	0.023
K	2 59	2 89	0.102	0.114
L	0 89	1 27	0 035	0.050
S	5 21	5 46	0.205	0.215
U	0 51	—	0.020	—
V	0 77	1 14	0.030	0.045
W	0.84	0 94	0.033	0.037
Y	4 32	–	0.170	—
Z	3 69	—	0.145	—

CASE 369A-04
MTD3055EL



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	·1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369-03
MTD3055EL-1

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MOTOROLA

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GENERAL INSTRUMENT

AY-3-1015D

UAR/T: Universal Asynchronous Receiver/Transmitter

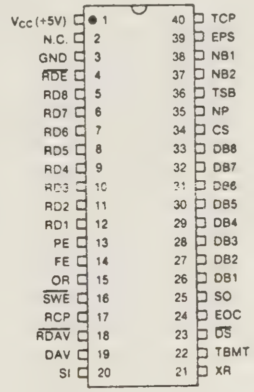
FEATURES

- DTL and TTL compatible—no interfacing circuits required—drives one TTL load
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation—can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs—bus structure capability
- Low Power—minimum power requirements
- Input Protected—eliminates handling problems

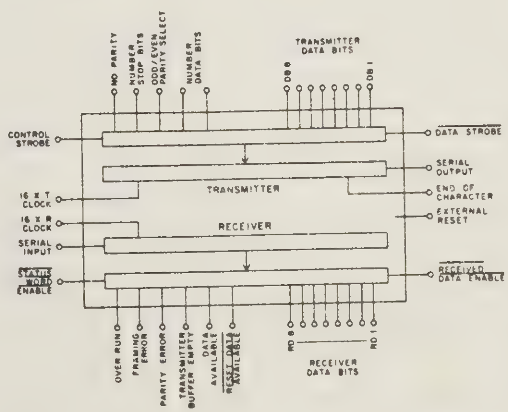
AY-3-1015D
- Single Supply Operation: +4.75V to +5.25V
- 1½ stop bit mode
- External reset of all registers except control bits register
- N-channel Ion Implant Process
- 0 to 25K baud
- Pull-up resistors to V_{CC} on all inputs

PIN CONFIGURATION
40 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, 1, 1½, or 2 stop bit capability, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	N.C.	(Not connected)
3	Ground	Ground
4	$\overline{\text{Received Data Enable}}$ ($\overline{\text{RDE}}$)	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{\text{RDE}}$ is "0" and a high impedance state when $\overline{\text{RDE}}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	$\overline{\text{Status Word Enable}}$ ($\overline{\text{SWE}}$)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	$\overline{\text{Reset Data Available}}$ ($\overline{\text{RDAV}}$)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 8.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 7, 8.
21	External Reset (XR)	Resets all registers. Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 14, 16.
23	$\overline{\text{Data Strobe}}$ ($\overline{\text{DS}}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{\text{DS}}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 13, 15.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with Respect to GND) .... −0.3V to +16V
Storage Temperature .... −65°C to +150°C
Operating Temperature .... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) .... +330°C

Standard Condition (unless otherwise noted):
V_{CC} = +4.75V to +5.25V
Operating Temperature (T_A) = 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic Levels (AY-3-1015)					
Logic 0	0	—	0.8	Volts	
Logic 1	2.0	—	V_{CC}+0.3	Volts	Has internal pull-up resistors to V_{CC}.
Input Capacitance					
All inputs	—	—	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL} = 1.6mA (sink)
Logic 1	2.4	—	—	Volts	I_{OH} = −40μA (source)—at V_{CC} = +5V
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig. 19
Power Supply Current					
I_{CC} at V_{CC} = +5V	—	10	15	mA	See Fig. 21

Standard Conditions (unless otherwise noted)

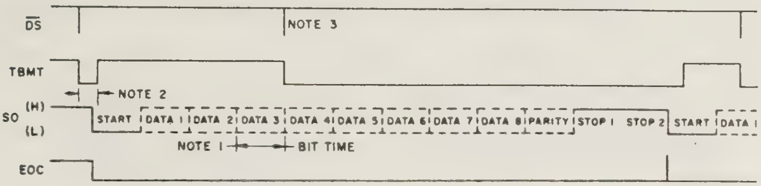
T_A = 25°C, Output load capacitance 50pF max.

AC CHARACTERISTICS

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	DC	—	400	kHz	at V_{CC} = +4.75V
Baud	0	—	25	kbaud	at V_{CC} = +4.75V
Pulse Width					
Clock Pulse	1.0	—	—	μs	See Fig. 5
Control Strobe	200	—	—	ns	See Fig. 11
Data Strobe	200	—	—	ns	See Fig. 10
External Reset	500	—	—	ns	See Fig. 9
Status Word Enable	500	—	—	ns	See Fig. 17
Reset Data Available	200	—	—	ns	See Fig. 18
Received Data Enable	500	—	—	ns	See Fig. 17
Set Up & Hold Time					
Input Data Bits	20	—	—	ns	See Fig. 10
Input Control Bits	20	—	—	ns	See Fig. 11
Output Propagation Delay					
TPD0	—	—	500	ns	See Fig. 17 & 20
TPD1	—	—	500	ns	See Fig. 17 & 20

**Typical values are at +70°C and nominal voltages.

TIMING DIAGRAMS



NOTE. SEE FIGURES 2, 3, 4 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

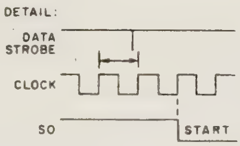


Fig. 1 UAR/T — TRANSMITTER TIMING

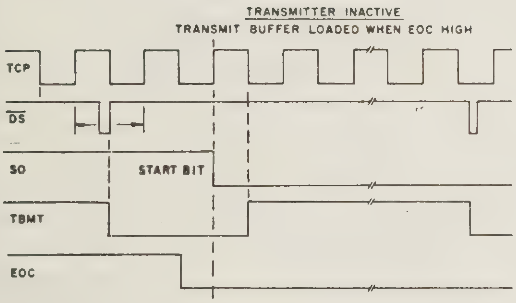


Fig. 2 TRANSMITTER AT START BIT NOT A TEST POINT

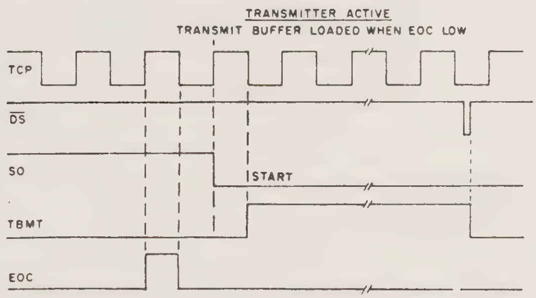
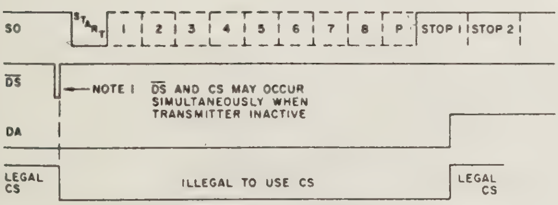
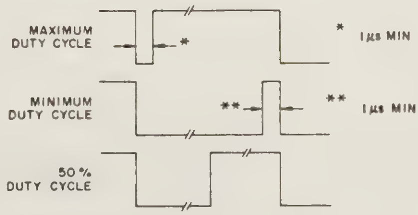


Fig. 3 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE, CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME.

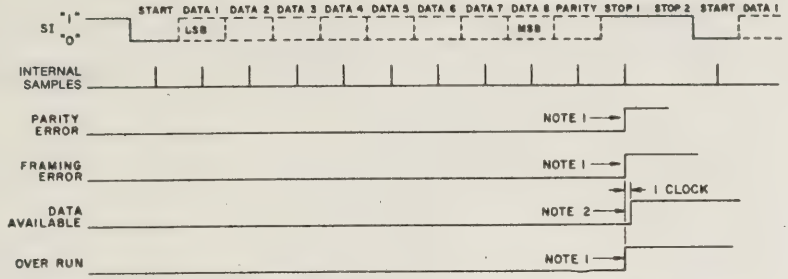
Fig. 4. ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig. 5 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Fig. 6 UAR/T — RECEIVER TIMING

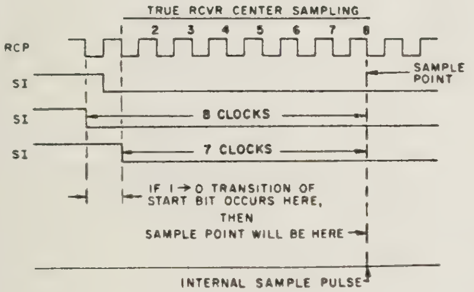


Fig. 7

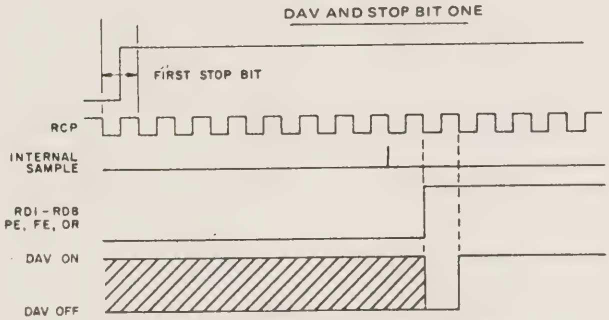
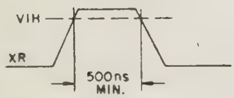


Fig. 8 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V.

Fig. 9 XR PULSE

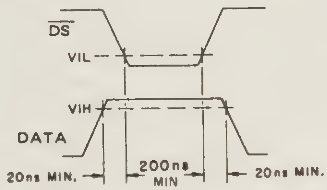
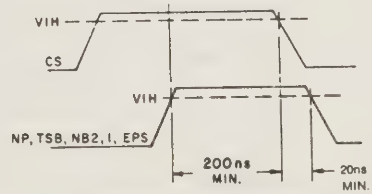
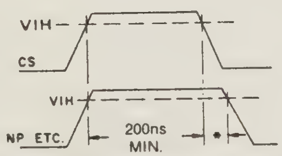


Fig. 10 $\overline{DS}$



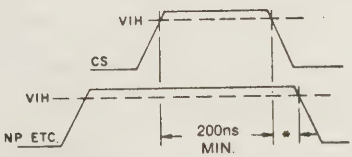
CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

Fig. 11a CS



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM.

Fig. 11b



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

* 20ns MIN.

Fig. 12

TIMING DIAGRAMS

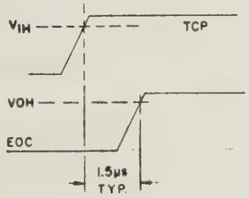


Fig. 13 EOC TURN-ON

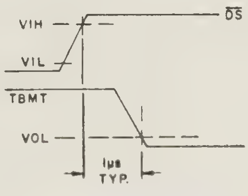


Fig. 14 TBMT TURN-OFF

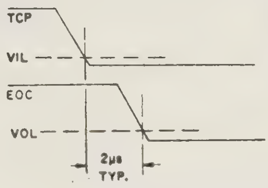


Fig. 15 EOC TURN-OFF

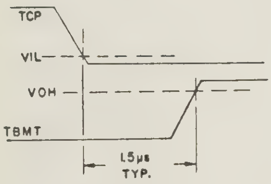


Fig. 16 TBMT TURN-ON

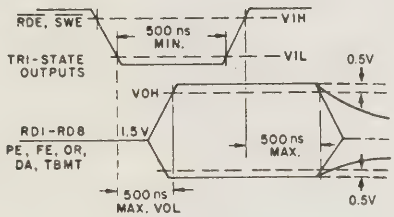


Fig. 17 RDE, SWE

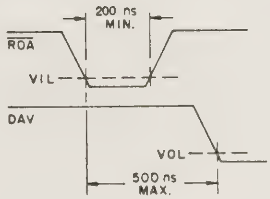


Fig. 18 RDAV

TYPICAL CHARACTERISTIC CURVES

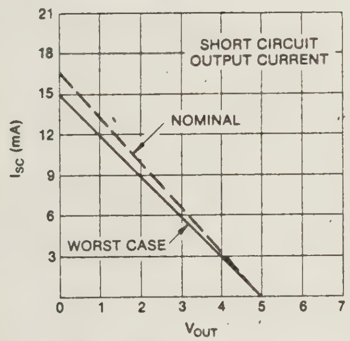


Fig. 19 SHORT CIRCUIT OUTPUT CURRENT
(only 1 output may be
shorted at a time)

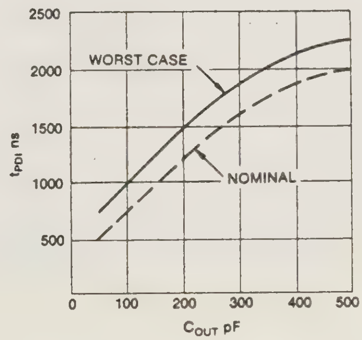


Fig. 20 RD1-RD8, PE, FE, OR, TBMT, DAV

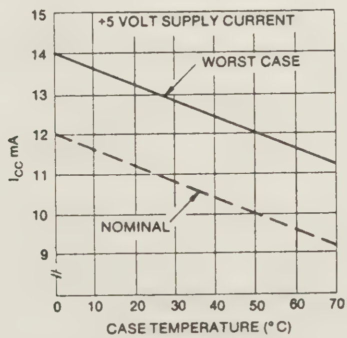


Fig. 21 +5 VOLT SUPPLY CURRENT

UAR/T: Universal Asynchronous Receiver/Transmitter

TRANSMITTER OPERATION

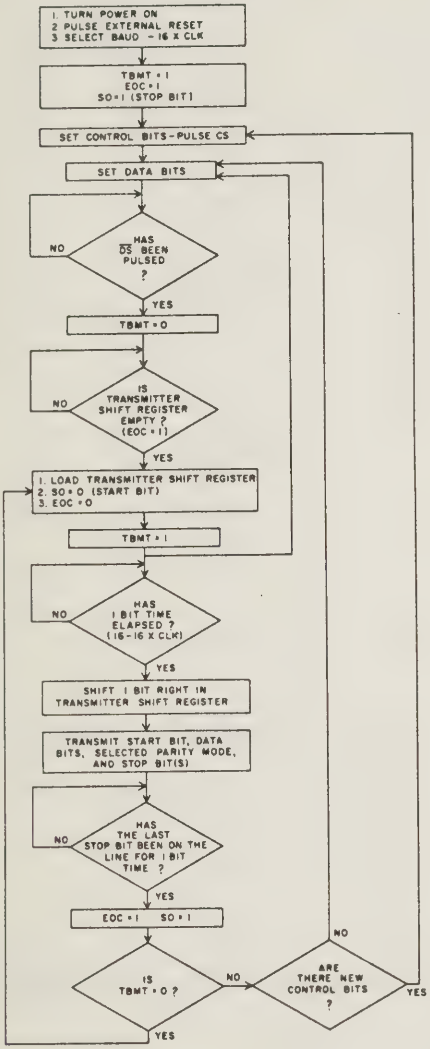


Fig. 23

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

RECEIVER OPERATION

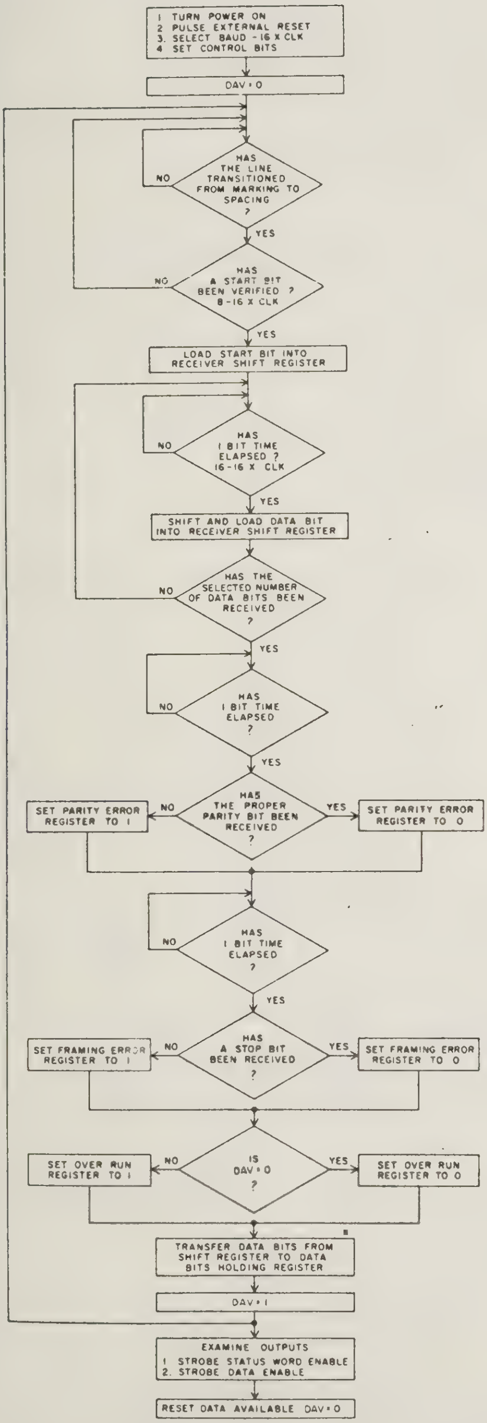


Fig. 24

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

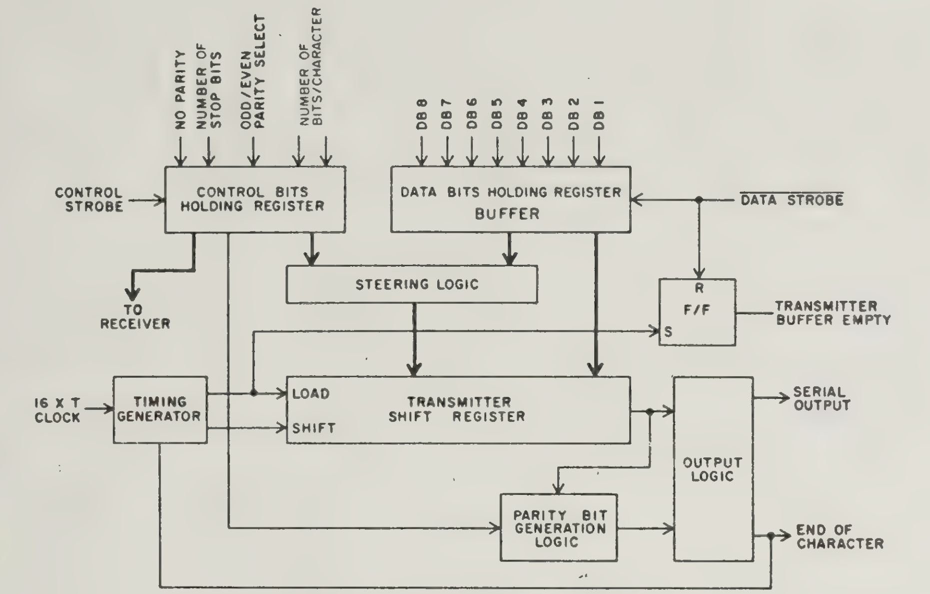


Fig. 25 TRANSMITTER BLOCK DIAGRAM

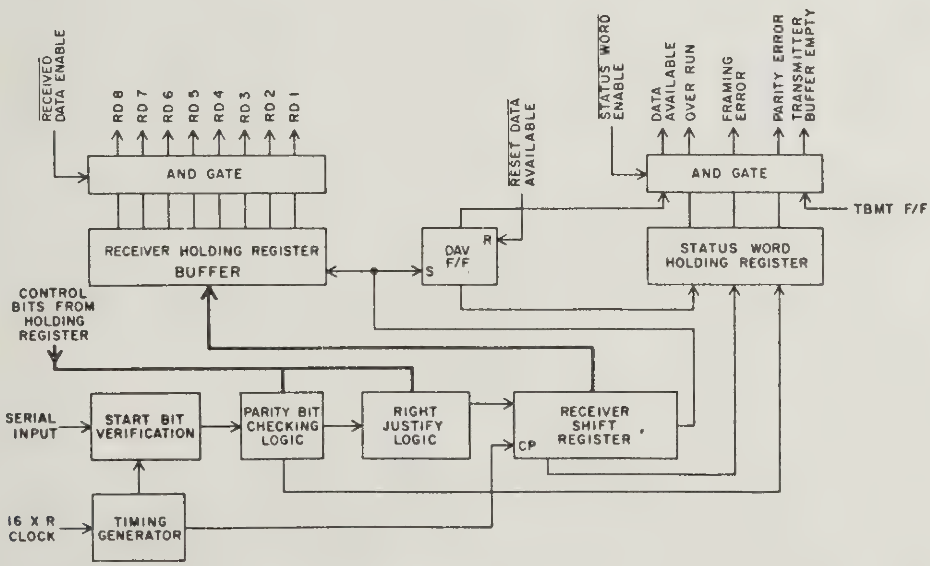


Fig. 26 RECEIVER BLOCK DIAGRAM

Parko

PARTS LIST AND TRACEABILITY RECORD

Page 1 of 2

Date 3-16-89 Parko P/N 101847- OPTICAL LINK RECEIVER Rev. ______ S/N ______

Ref. Des.	P/N	Description	Unit Qty.	Total Qty	Insp	Manufacturer	Parko PO	Notes
	HU-8830-1.250 HU-8830-CA	CAN COVER } TIN DIP	1 1			HUDSON		
		LABEL	1					
		P.C. BOARD	1					
		POTTING 160-1						
U1	MC78L05CT	5V REGULATOR	1			MOTO - OR EQUIVALENT		
U2	AY-3-1015D	UART	1			GI		
U3	SN74HC4060N	OSCILLATOR/DIVIDER	1			TI - OR EQUIV.		
U4	CD4098BE	DUAL ONE SHOT	1			RCA OR EQUIV.		
U5	CD4002BE	DUAL 4 IN	1			RCA OR EQUIV.		
U6	CD4001BE	QUA 2 IN	1			RCA OR EQUIV.		
U7-U8	CD40174BE	FLIP FLOP LATCH	2			RCA OR EQUIV.		
U9	CD4075BE	TRIPPLE 3 IN	1			RCA - OR EQUIV		
Q1-Q2	2N4123	XTOR	2			MOTO - OR EQUIV.		
Q3-Q16	MTD3055EL1	MOSFET	14			MOTORO.		
CR1	P6KE22	SUPPRESOR ZENER	1			MOTOR. OR EQUIV.		
CR2	MFOD3100	PIN PHOTO DIODE	1			MOTOROLA.		
CR3	L59D-R2-W	LED INDICATOR	1			LEECRAFT/NEWARK		
X1	ME-332-1033	3.2768 MHZ XTAL	1			MOUSER		

Parko

PARTS LIST AND TRACEABILITY RECORD

Sheet 2 of 2

Date 3-16-89 Parko P/N 101847-OPTICAL LINK RECEIVER Qty. ____ S/C ______

Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PO	Notes
F1	44FP049	.5 A FUSE-STANDARD	1			MOUSER		
	~~44FP...~~	IN LINE FUSE HOLDER	1			MOUSER		
R1	RC07GF~~474~~K 154	~~470K~~ 150K - RESISTOR						
R2	RC07GF101K	100 Ω "						
R3 - R6	RC07GF103K	10K "	2					
R4	RC07GF223K	22K "	1					
R5	RC07GF226K	22MEG "	1					
R7	RC07GF104K	100K "	1			(NEED 5-10 OHMS) REVIEW THIS VALUE		
R8	RC07GF121K	120 Ω "	1					
C1	540-1.0M35	1UF/35V - CAP	1			MOUSER-MATSUO		
C2	540-4.7M10	4.7UF/10V CAP	1			" "		
C3-C6	CK12BX103K.	.01/50V CAP	2					
C4-C5	21RD722	22PF/35V CAP	2			MOUSER		
C7	540-0.22M35	.22UF/35V CAP	1			MOUSER-MATSUO		
J1	905-145-5000	FIBER OPTICS RECEPTACLE	1			AMPHENOL		
	G-403	GROMET (3/8 HOLE)(1/4)	1			WALDON		
	AWG-22	WIRIES	16					

Parko
ELECTRONICS CO. INC.

PARTS LIST AND TRACEABILITY RECORD

Date 3-16-89 Parko P/N 101847- OPTICAL LINK RECEIVER Qty. ____ S/O ____

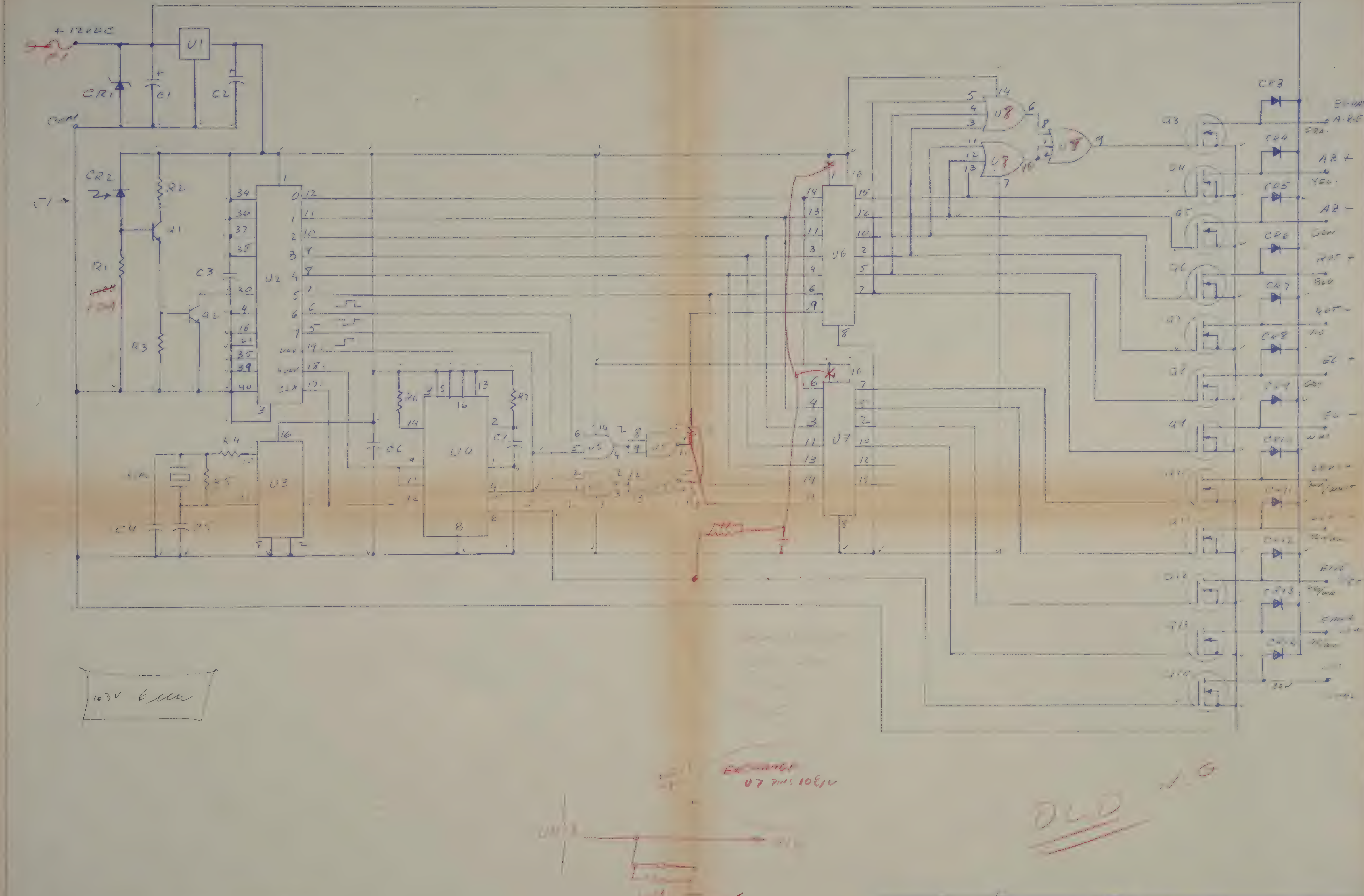
Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PO	Notes
	HU-8830-1.250 HU-8830-CA	CAN COVER } TIN DIP	1 1			HUDSON		
		LABEL	1					
		P.C. BOARD	1					
		POTTING 160-1						
U1	MC7805CT	5V REGULATOR	1			MOTO - OR EQUIVALENT		
U2	AY-3-1015D	UART	1			GI		
U3	SN74HC4060N	OSCILLATOR/DIVIDER	1			TI - OR EQUIV.		
U4	CD4098BE	DUAL ONE SHOT	1			RCA OR EQUIV.		
U5	CD4002BE	DUAL 4IN	1			RCA OR EQUIV.		
U6	CD4001BE	QUA 2IN	1			RCA OR EQUIV.		
U7-U8	CD 40174BE	FLIP-FLOP LATCH	2			RCA OR EQUIV.		
U9	CD4075BE	TRIPPLE 3IN	1			RCA - OR EQUIV		
Q1-Q2	2N4123	XTOR	2			MOTO - OR EQUIV.		
Q3-Q16	MTD3055EL1	MOSFET	14			MOTORO.		
CR1	P6KE22	SUPPRESOR ZENER	1			MOTOR. OR EQUIV.		
CR2	MFOD3100	PIN PHOTO DIODE	1			MOTOROLA.		
CR3	L59D-R2-W	LED INDICATOR	1			LEECRAFT/NEWARK		
X1	ME-332-1033	3.2768 MHZ XTAL	1			MOUSER		

Parko
ELECTRONICS CO. INC.

PARTS LIST AND TRACEABILITY RECORD

Date 3-16-89 Parko P/N 101847-OPTICAL LINK RECEIVER Qty. ______ S/C ______

Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PO	Notes
F1	44FP049	.5 A FUSE-STANDARD	1			MOUSER		
	~~[illegible]~~	IN LINE FUSE HOLDER	1			MOUSER		
R1	RC07GF474K	470K- RESISTOR						
R2	RC07GF101K	100 Ω "						
R3-R6	RC07GF103K	10K "	2					
R4	RC07GF223K	22K "	1					
R5	RC07GF226K	22MEG. "	1					
R7	RC07GF104K	100K "	1			(NEED 5-10 MΩS) REVIEW THIS		VALUE
R8	RC07GF121K	120 Ω "	1					
C1	540-1.0M35	1UF/35V - CAP	1			MOUSER-MATSUO		
C2	540-4.7M10	4.7UF/10V CAP	1			" "		
C3-C6	CK12BX103K.	.01/50V CAP	2					
C4-C5	21RD722	22PF/35V CAP	2			MOUSER		
C7	540-0.22M35	.22UF/35V CAP	1			MOUSER-MATSUO		
J1	905-145-5000	FIBER OPTICS RECEPTACLE	1			AMPHENOL		
	G-403	GROMET (3/8 HOLE)(1/4)	1			WALDON		
	AWG-22	WIRES	16					



3. PARTS LIST: PL101847
2. ASSEMBLY: 101847
1. TOP DRAWING: 101847
NOTES:

DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR		1-4-78
	CHK		
TOLERANCES (unless otherwise specified)	DSGN		
.X ±.1	PROJ		
.XX ±.03	REL		
.XXX ±.010	APPROVED		
ANGLES ±0.5°	APPROVED		
MACH SURF ✓	DO NOT SCALE DRAWING		

Parko ELECTRONICS COMPANY INC., SANTA ANA, CALIF.

OPTICAL LINK RECEIVER

CODE IDENT NO.	SIZE		REV
13979		101848	
SCALE		SHEET OF	

Parko

PARTS LIST AND TRACEABILITY RECORD

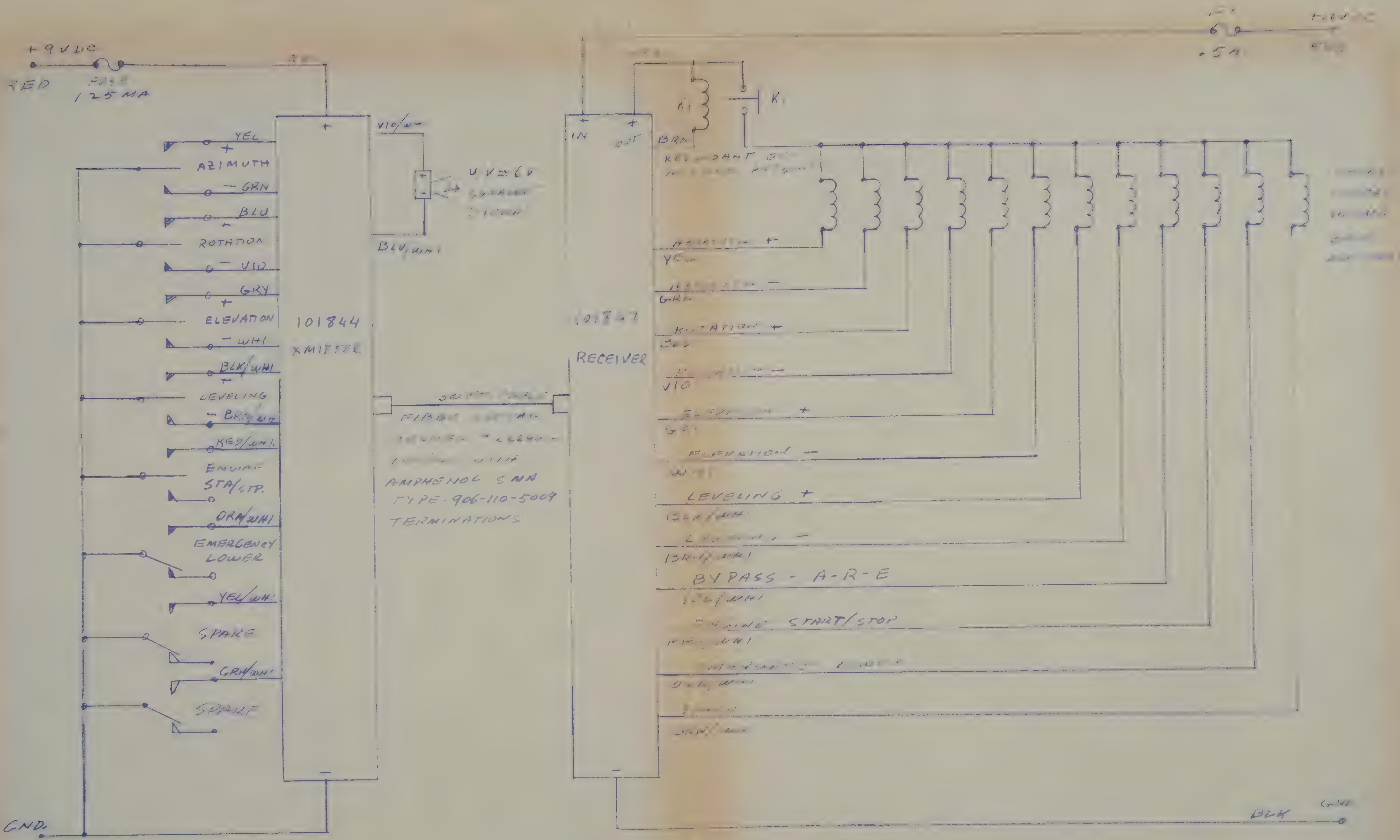
Sheet 1 of 2

Date 1-4-89 Parko P/N: 101847 - RECEIVER

Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PO	Notes
	HU-8830-1.250 HU-8830-CA	CAN COVER } TIN DIP	1 1			HUDSON		
		P.C. BOARD	1					
U1	MC78L05CT	5 VOLT REGULATOR	1			MOT		
U2	AY-3-1015D	UART	1			GI		
U3	SN74HC4060N	OSCILLATOR/DIVIDER	1			RCA		
U4	CD4098BE	DUAL ONE SHOT	1			RCA		
U5	CD4011BE	QUAD DUAL NAND	1			RCA		
U6, U7	CD40174BE	FLIP-FLOP	1			RCA		
U8	CD4075BE	TRIPLE 3 INPUT OR	1			RCA		
Q1, Q2	2N4123	XTOR	2			MOT		
Q3 → Q14	MTP15N05L	MOSFET XTOR	12			MOT		
CR1	P6KE22	SUPPRESSOR	1			MOT		
CR2	MFOD3100	PIN PHOTO DIODE	1			MOT		
CR3 - CR14	1N4002	DIODE	12					

SEE REVISED LIST

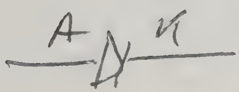
ADD [illegible] RES - [illegible] - [illegible] CAP

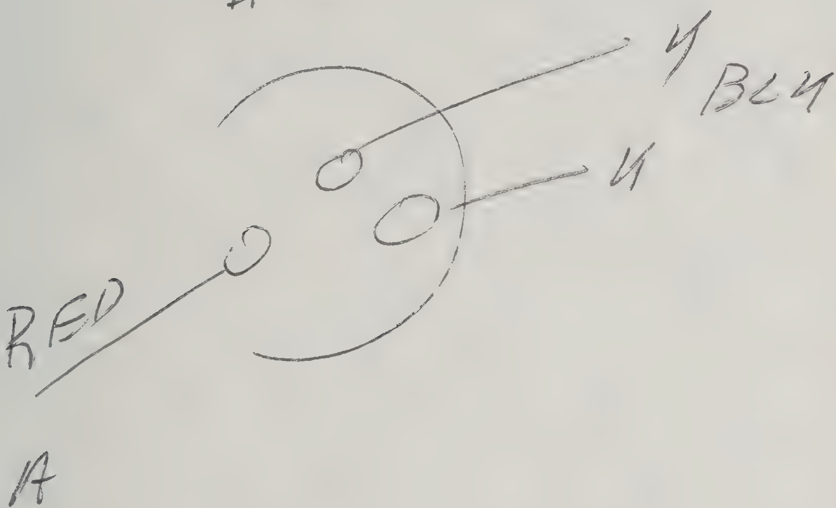


101863 - CONNECTION DIAGRAM - OPTICAL LINK
101844 AND 101867

PARKO ELECTRONICS
3-17-89

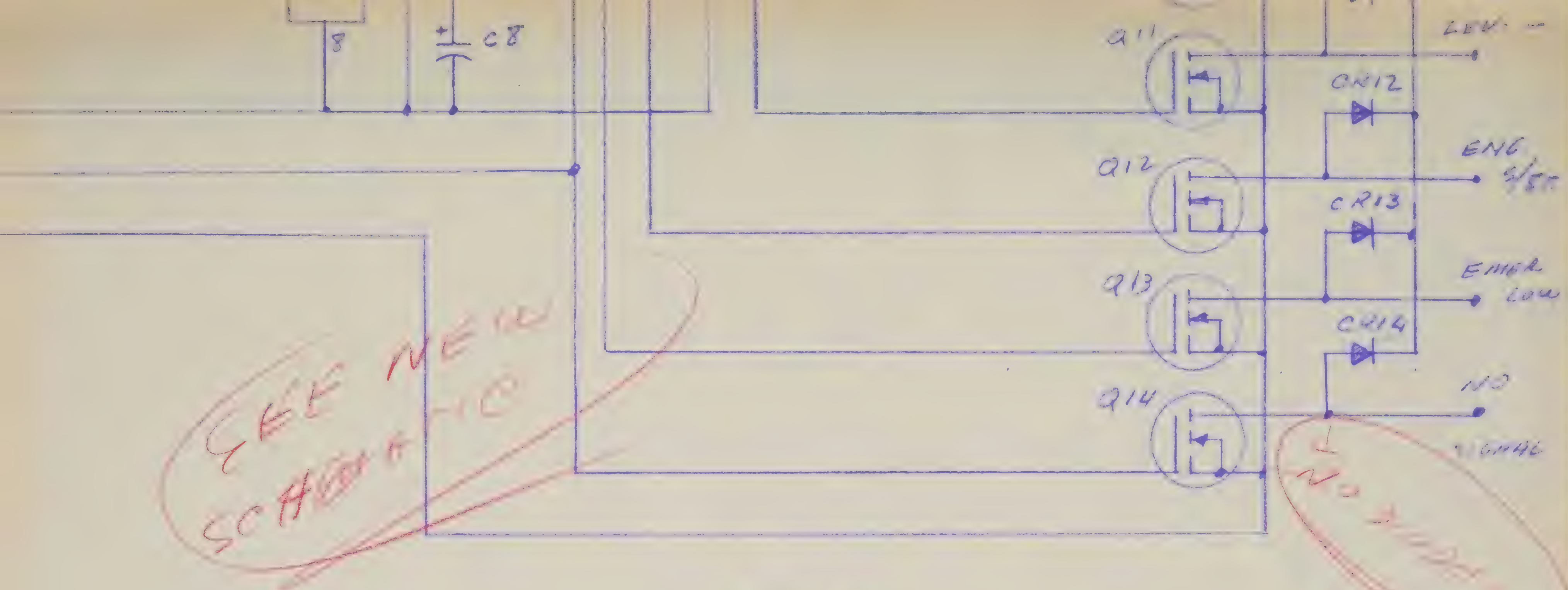
CR2





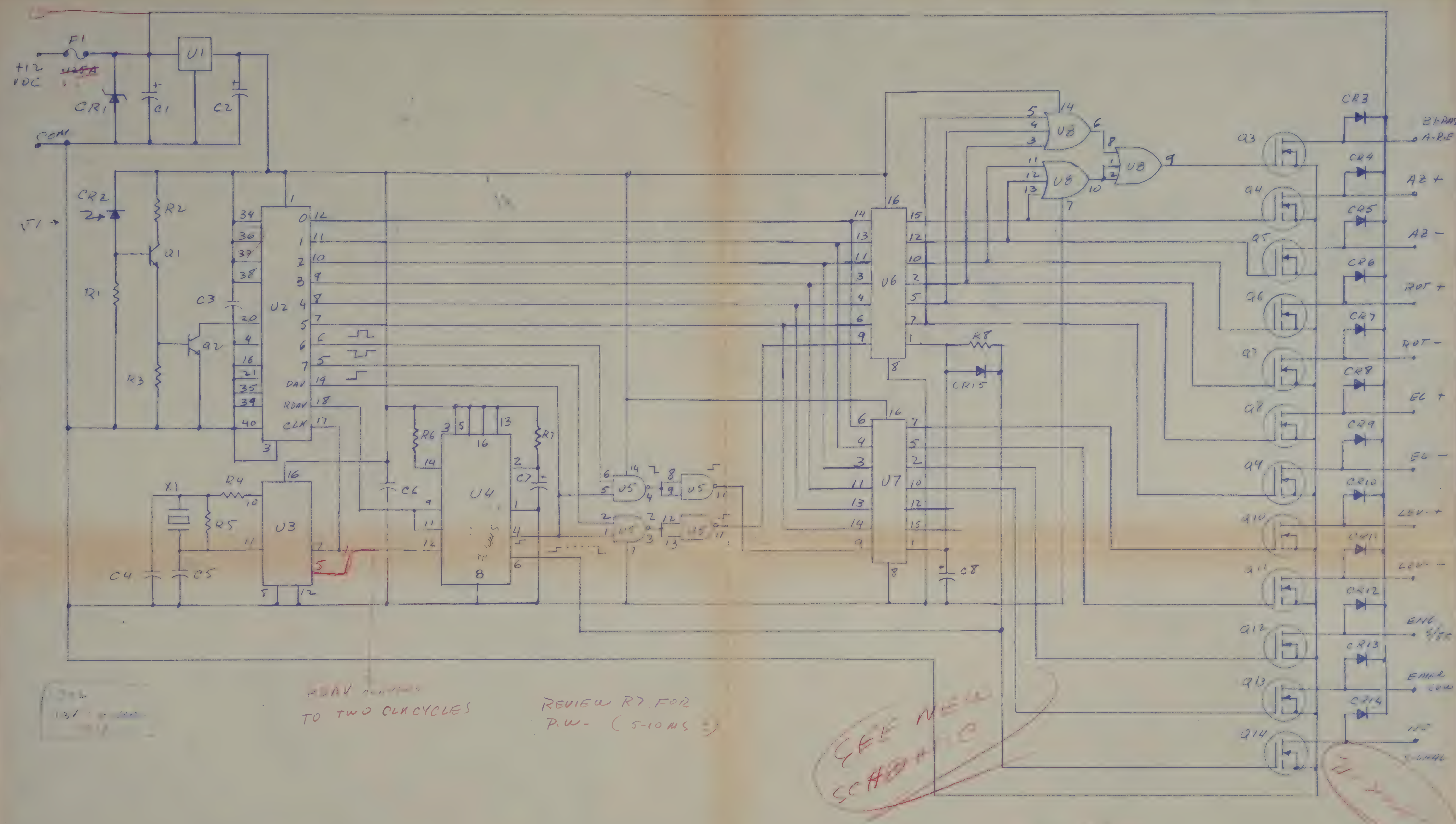
RED TO Q1

BLK - TO +5V



11 INDEPENDENT OUTPUTS
PLUS NO SIGNAL AND BY

DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR		**Parko** ELECTRONICS COMPANY INC., SANTA ANA, CALIF.
TOLERANCES (unless otherwise specified) .X ±.1 .XX ±.03 .XXX±.010 ANGLES±0.5°	CHK		OPTICAL LINK RECEIVER
	DSGN		
	PROJ		
	REL		
	APPROVED		CODE IDENT NO. 13979 | SIZE | 101848 | REV
MACH SURF ✓	APPROVED		
	DO NOT SCALE DRAWING		SCALE | SHEET OF



RDAV ... TO TWO CLKCYCLES

REVIEW R7 FOR P.W. (5-10MS ?)

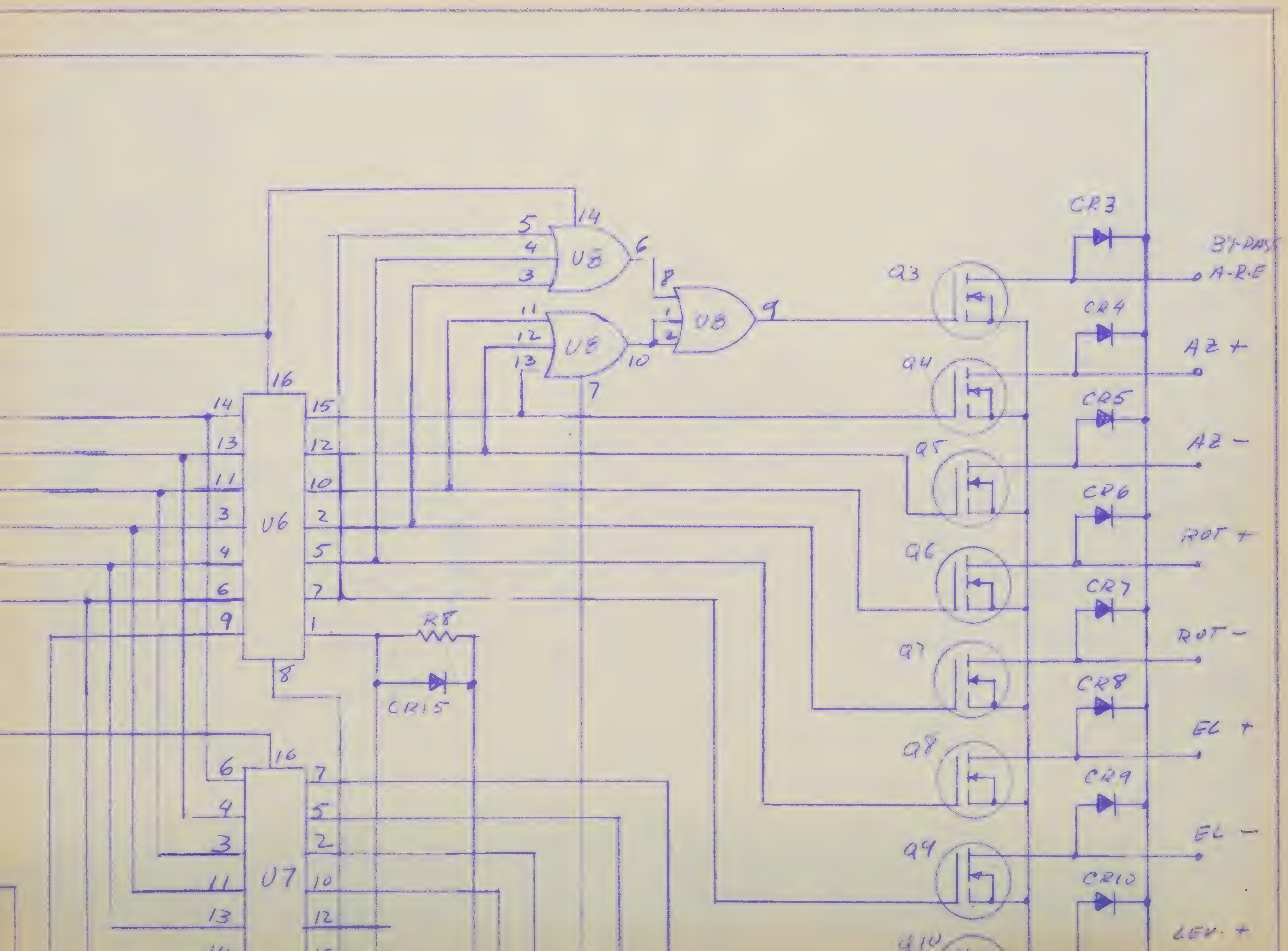
SEE NEW SCHEMATIC

11 INDEPENDENT OUTPUTS

PLUS NO ...

4. INTERCONNECTING DIAGRAM 101863
3. PARTS LIST: PL101847
2. ASSEMBLY: 101849
1. TOP DRAWING: 101847
NOTES:

DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR	**Parko** ELECTRONICS COMPANY INC., SANTA ANA, CALIF.
TOLERANCES (unless otherwise specified) .X ±.1 .XX ±.03 .XXX ±.010 ANGLES ±0.5°	CHK	
	DSGN	OPTICAL LINK RECEIVER
	PROJ	
	REL	
	APPROVED	CODE IDENT NO. 13979 — SIZE — 101848 — REV
MACH SURF ✓	APPROVED	
	DO NOT SCALE DRAWING	SCALE — SHEET — OF



BY-PASS
A-R-E
AZ +
AZ -
ROT +
ROT -
EL +
EL -
CR3
CR4
CR5
CR6
CR7
CR8
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CR10
Q3
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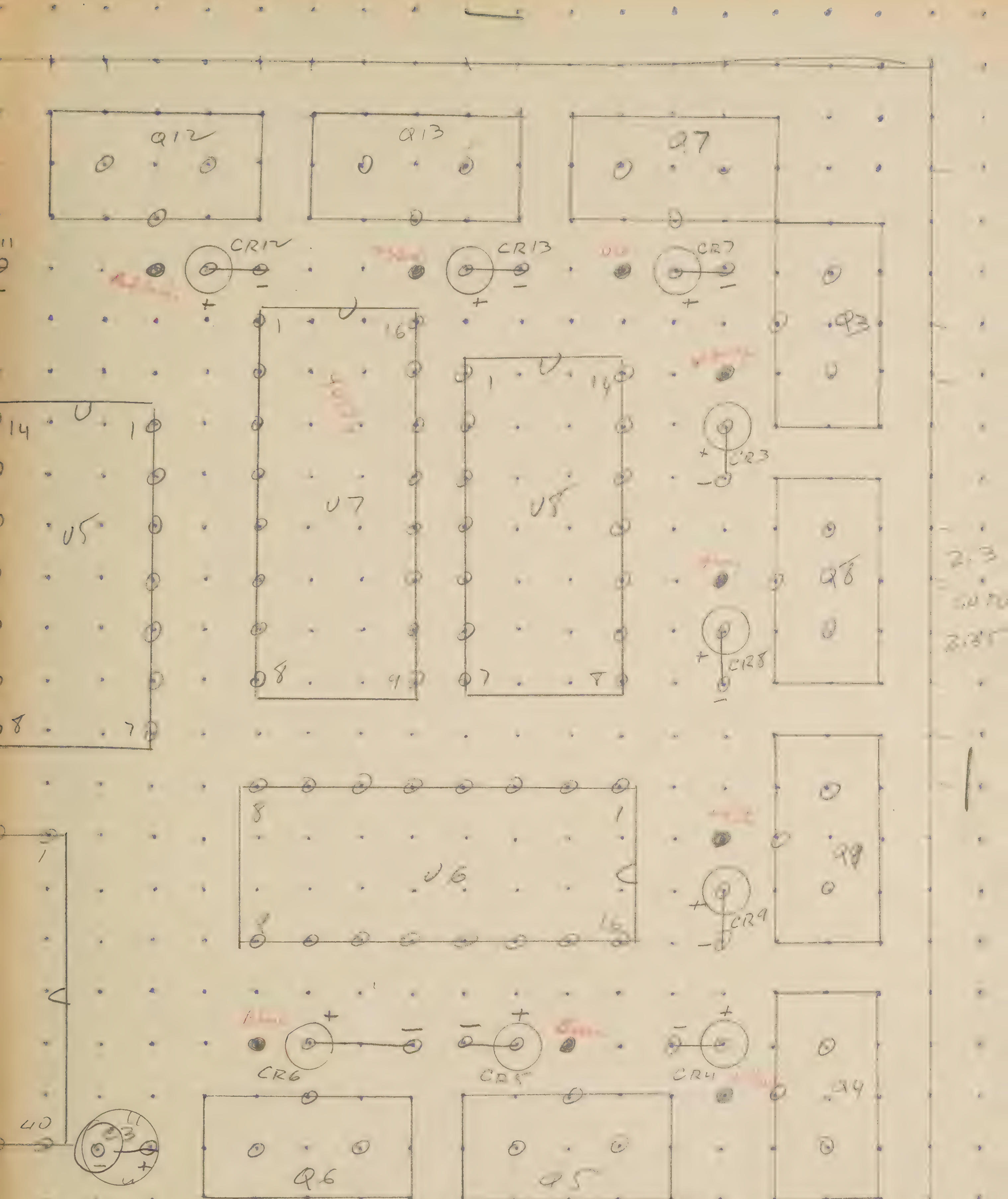
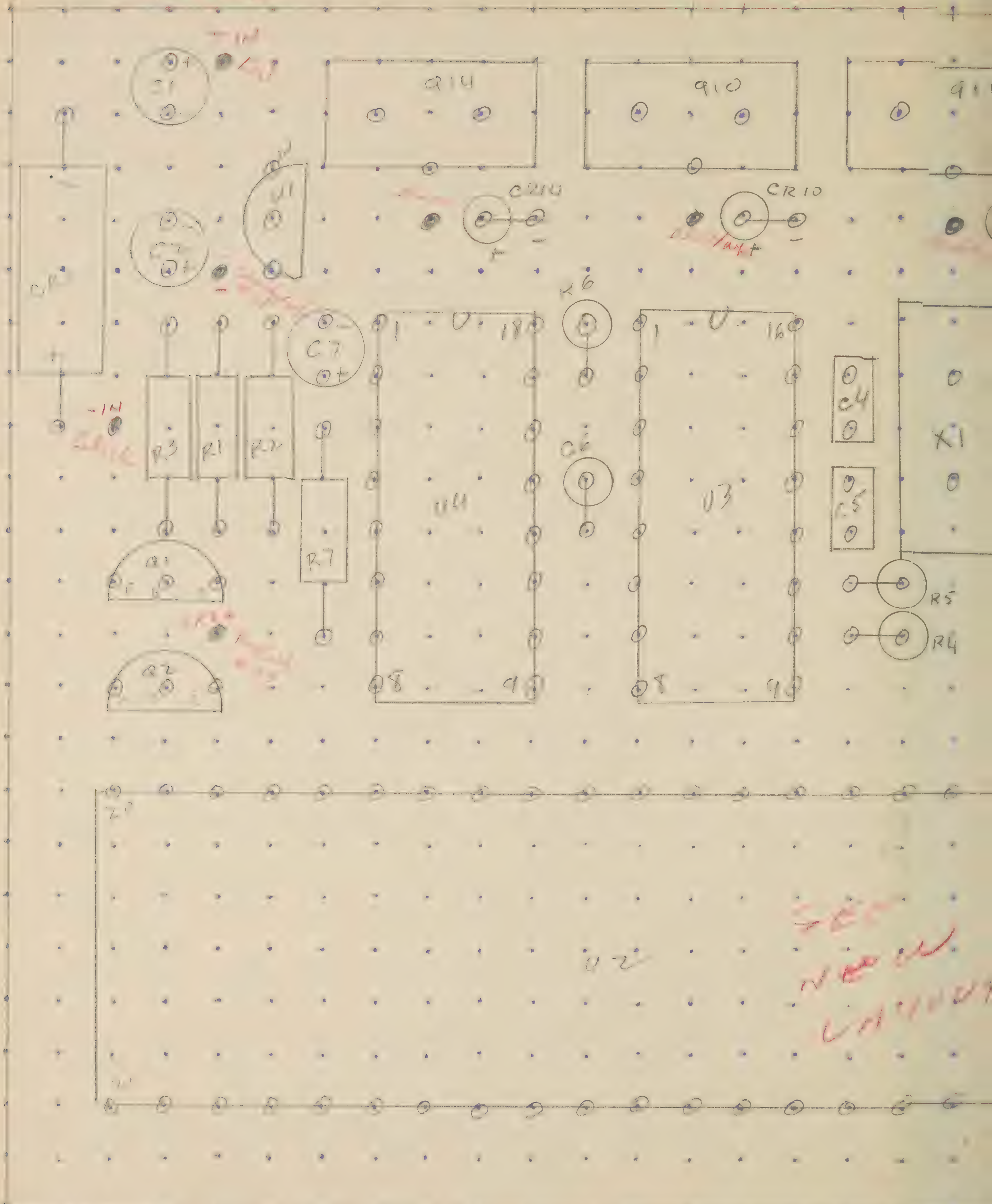
U8
U6
U7
R8
CR15



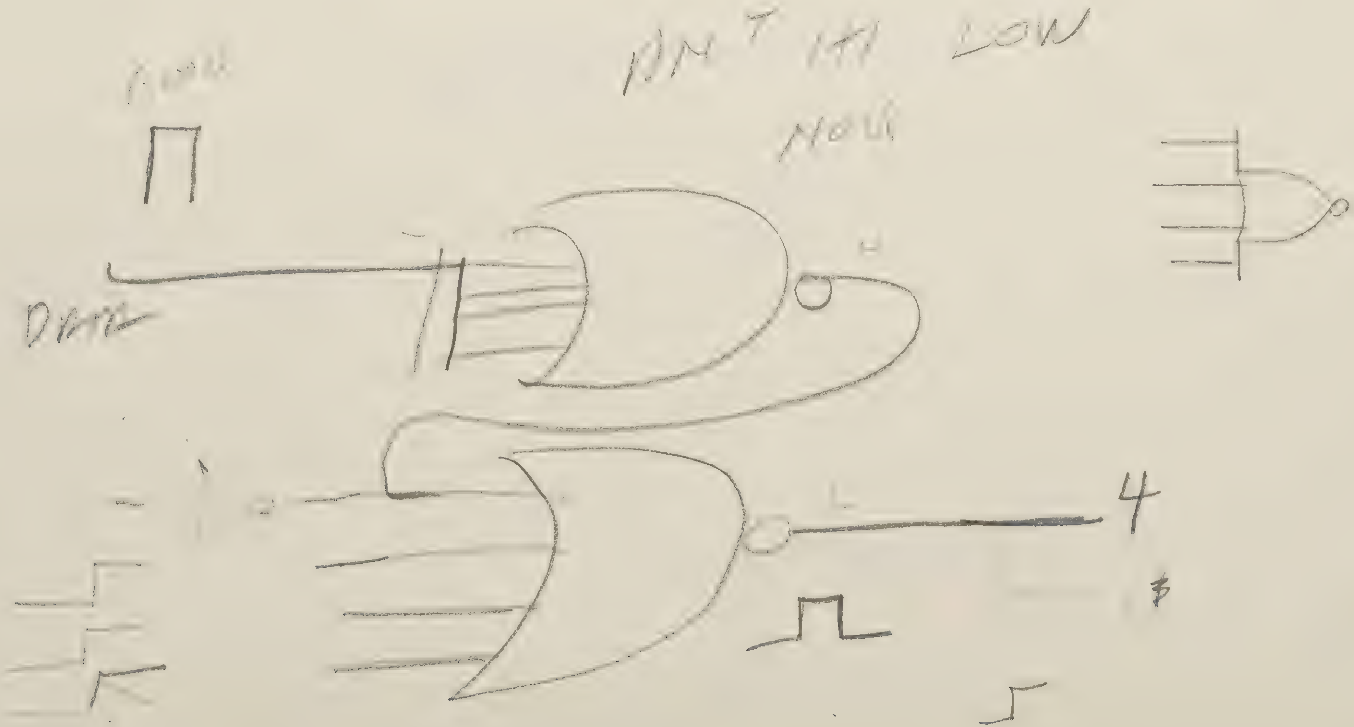
ASSY- RECEIVER 3,5 C0-6385 1-12-79

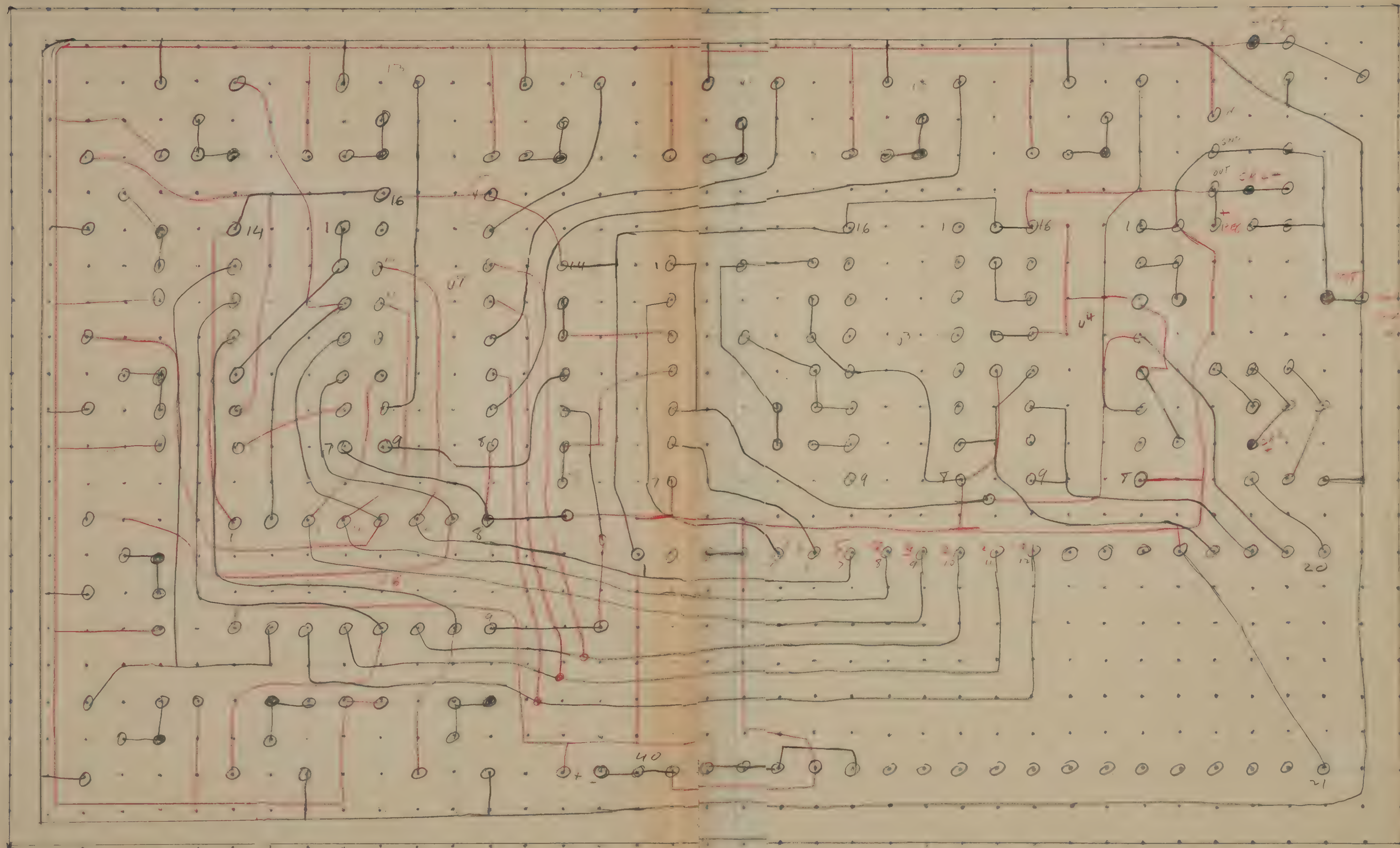
Power
#20 ga

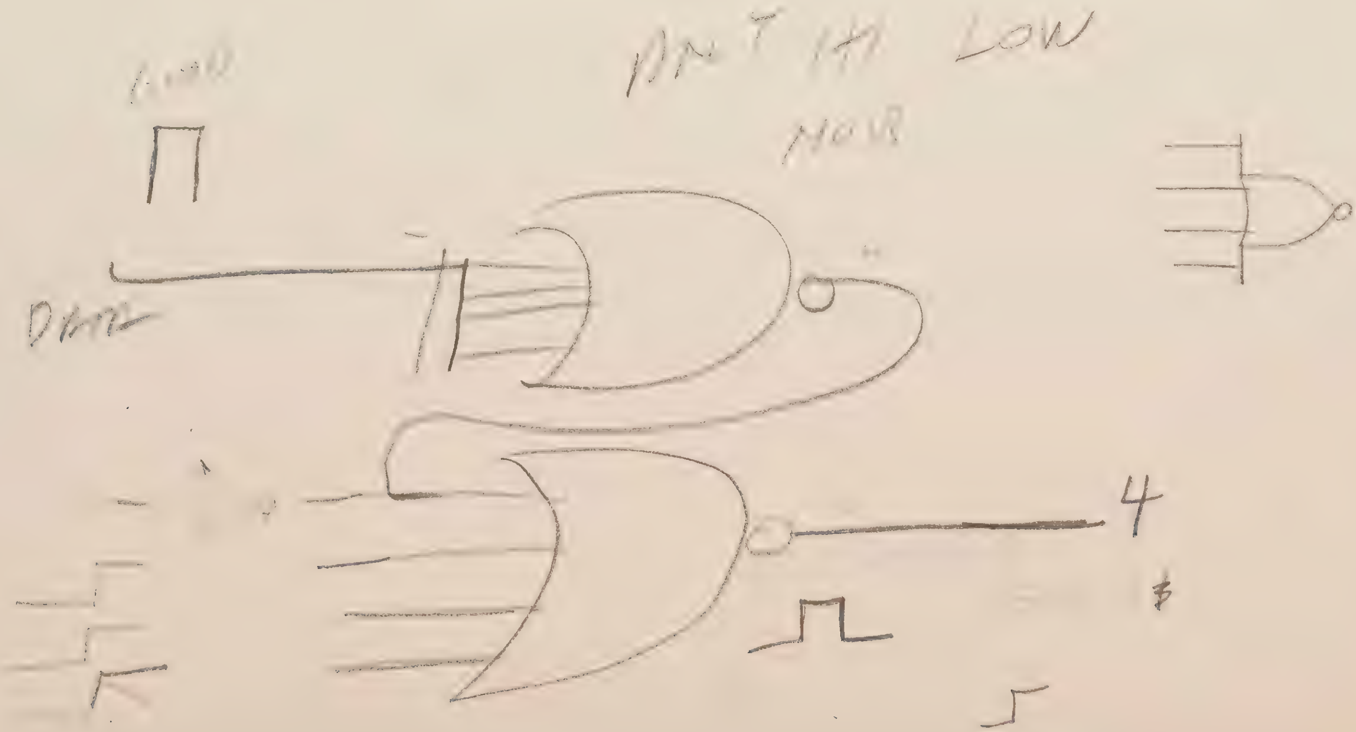
#22 ga



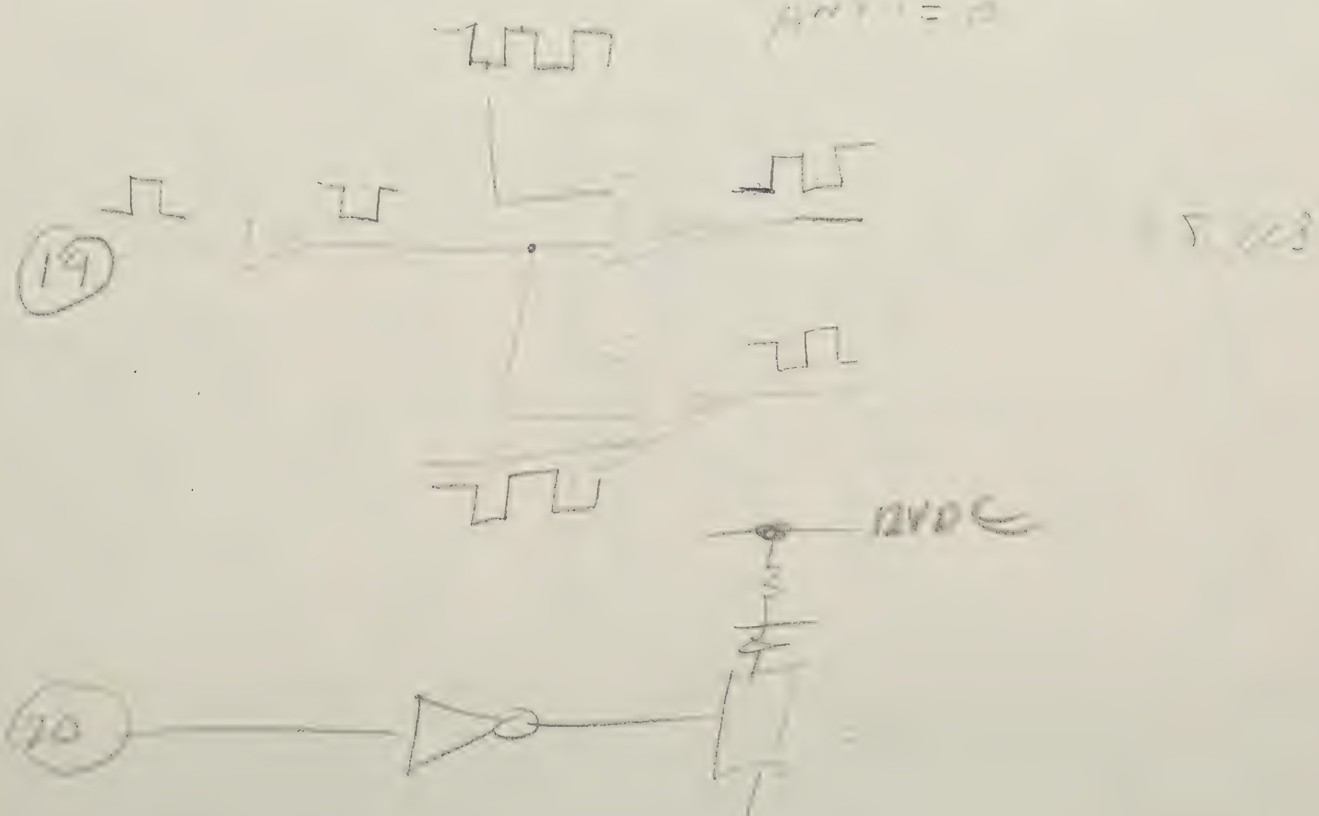
10/84


LOW
4

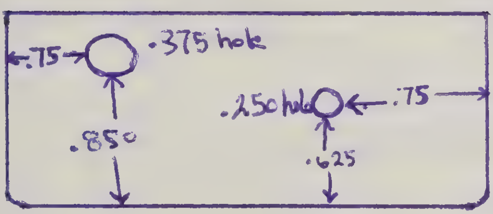




NOR
4


19
12VDC
20

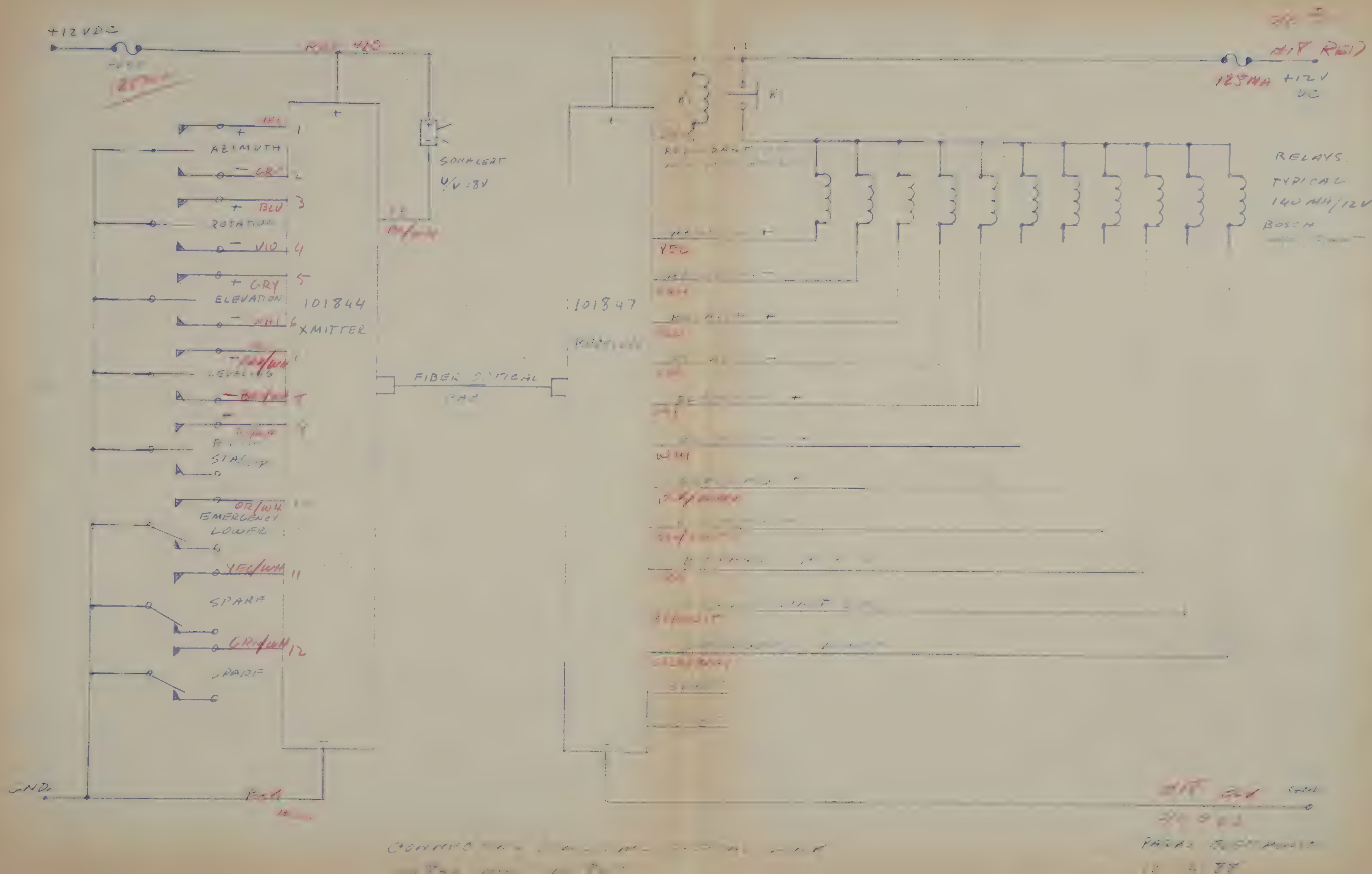
2-1-89



Both holes on
Same END

RECEIVER CAN

10847


+12VDC
FUSE
SONALERT
V/V = 8V
AZIMUTH
ROTATION
ELEVATION
LEVELING
EMERGENCY
LOWER
SPARE
SPARE
GRY
BLU
VIO
GRY
OR/WH
YEL/WH
GRY/WH
101844
XMITTER
FIBER OPTICAL
101847
YEL
WHT
RELAYS
TYPICAL
140 MA/12V
BOSCH
#18 RED
125 MA
+12V
DC
GND

Parko

PARTS LIST AND TRACEABILITY RECORD

Sheet 1 of 2

Date JAN-31-89 Parko P/N 101847-OPTICAL LINK RECEIVER No. ______ S/O ______

Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PO	Notes
	HU-8830-1.250 HU-8830-CA	CAN COVER } TIN DIP	1 1			HUDSON		
		LABEL						
		3.85 x 2.35 P.C. BOARD	1					
		POTTING-160-1						
U1	MC78L05CT	5V REGULATOR	1			MOTO.		
U2	AY-3-1015D	UART	1			G.I.		
U3	SN74HC4060N	OSCILLATOR/DIVIDER	1			T.I.		
U4	CD4098BE	DUAL ONESHOT	1			RCA		
U5	CD4011BE	QUAD 2-IN NAND	1			RCA		
U6-U7	CD40174BE	FLIP-FLOP LATCH	2			RCA		
U8	CD4075BE	TRIPPLE 3-IN OR	1			RCA		
Q1-Q2	2N4123	XTOR	2					
Q3-Q14	MTP4N05L	MOSFET XTOR	12			MOT		
CR1	P6KE22	SUPPRESOR	1			MOT		
CR2	MFOD3100	PIN PHOTO DIODE	1			MOT		
CR3-CR14	1N4002	DIODE	12					
CR15	1N4128	DIODE	1					

SEE NEW PARTS LIST

Parko
ELECTRONICS CO. INC

PARTS LIST AND TRACEABILITY RECORD

Date JAN-31-79 Parko P/N 101847- OPTICAL LINK RECEIVER Qty. ____ S/C ____

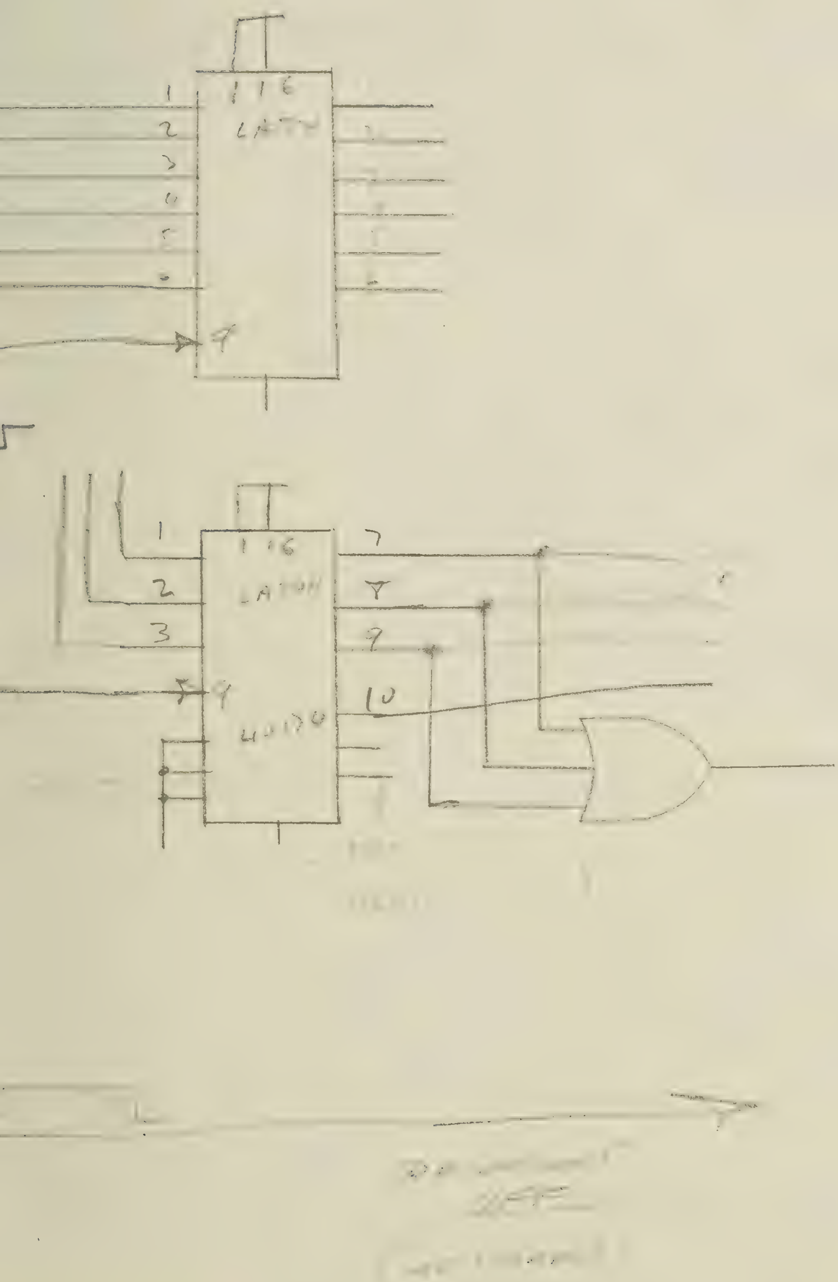
Ref. Des.	P/N	Description	Unit Qty	Total Qty	Insp	Manufacturer	Parko PC	Notes
X1	ME-332-1033	3.2768 MHZ XTAL	1			MOUSER		
F1		.125 A FUSE	1					
	44FH018	INLINE FUSE HOLDER	1			MOUSER		
R1, R8	RC07GF474K	470 K - RESISTOR	2					
R2	RC07GF101K	100 Ω - "	1					
R3-R6	RC07GF103K	10 K - "	2					
R4	RC07GF~~104~~ 223 K	~~100K~~ 22K - "	1					
R5	RC07GF226K	22M - "	1					
R7	RC07GF104K	100K - "	1					
C1	540-1.0M35	1UF/35V - CAP	1			MOUSER-MATSUO		
C2	540-4.7M10	4.7UF/10V "	1			" "		
C3-C6	CK12BX103K	.01UF/50V - "	2					
C4-C5	21RD722	22PF/50V "	2			MAUSER		
C7-C8	540-~~0.1M35~~	~~.1UF~~/35V "	2			MAUSER-MATSUO		
	[illegible]	[illegible]						
T1	905-145-5000	FIBER OPTICS RECEPTACLE	1			AMPHENOL		
	G-403	GROMET (3/8 HOLE)(1/4)	1			WALDON		
		WIRES	14					

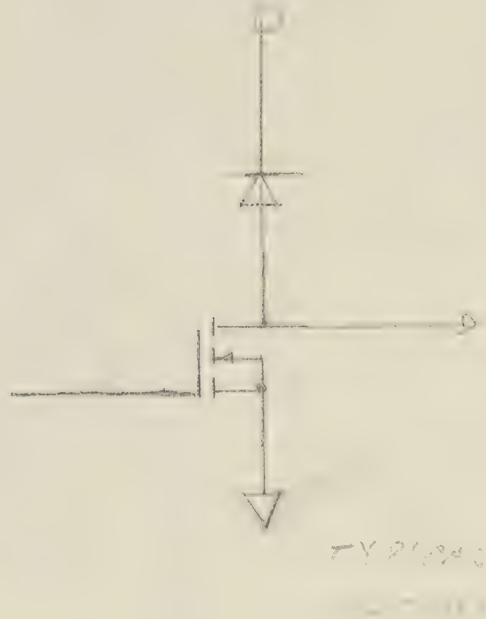
SHIP TO

GENERAL CABLE
APPARATUS DIVISION
5600 W 88th Ave
Westminster, CO 80030

Attn: Steve Epps

~~Littleton~~
Jefferson Co Airport





101847

[illegible]

[illegible]

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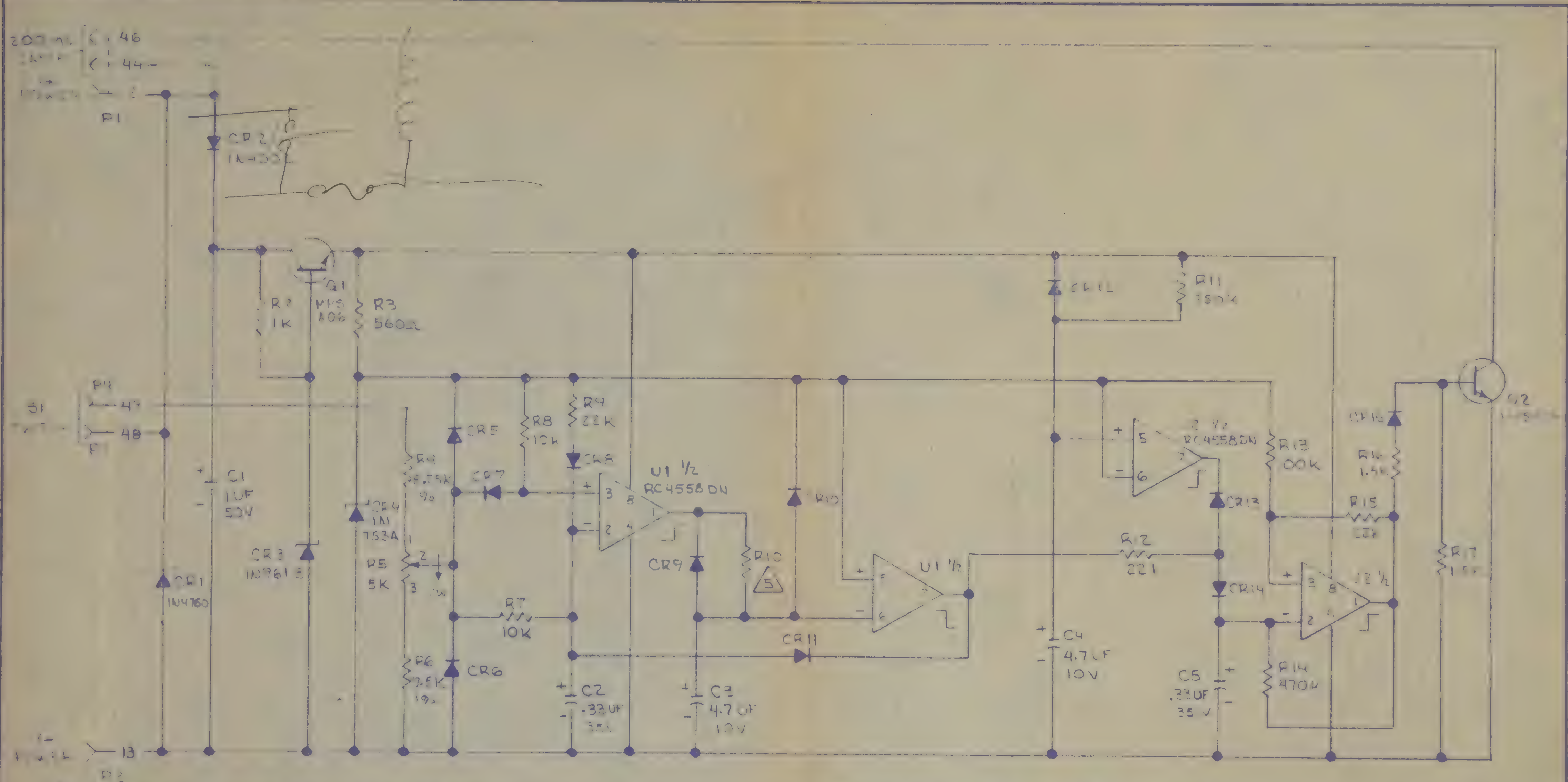


5 SELECTED AFTER ASSY PER ES900

4 R1 NOT USED

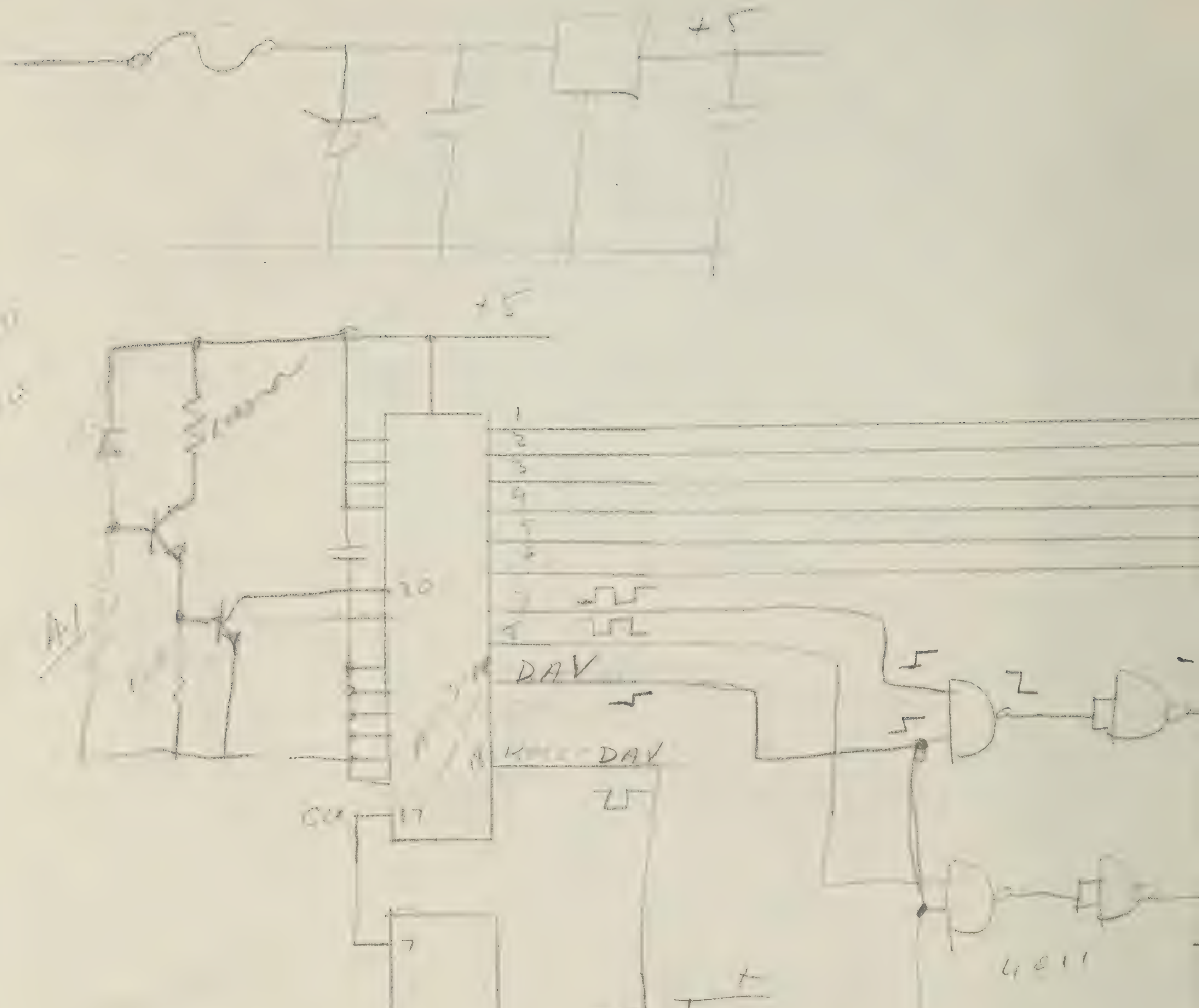
3 ALL DIODES ARE 1N4148 (EXCEPT AS NOTED)

2 ASSEMBLY: 101278

1 TOP DRAWING: 101296

NOTES:

DIMENSIONS ARE IN INCHES AND AFTER PLATING	DR	**Parko** ELECTRONICS COMPANY INC, SANTA ANA CALIF
TOLERANCES (unless otherwise specified) .X ±.1 .XX ±.03 .XXX ±.010 ANGLES ±0.5	CHK	SCHEMATIC — 12V BATTERY DISCHARGE MONITOR
	DSGN	
	PROJ	
	REL	
	APPROVED	CODE IDENT NO 13979 / SIZE B / 101277 / REV
MACH SURF ✓	APPROVED	
	DO NOT SCALE DRAWING	SCALE — / SHEET 2 OF 2


+5
DAV
CLK
4011

PARTS ON HAND

AY-3-1015D — 2

MC 3423 - O/V. — 5

74HC4060 - OSC/COUNT — 14

78L05 - REG. — 2

4082 - AND — 1 +

4503 - TRI-STATE BUFF — 12

40174 - LATCH — 2

15N05L - MOSFETS — 30

MFOE-3200 EMITER — 4

MFOD-3100 DETECTOR — 4

ME-332-1033 XTAL — 9

22PF FOR XTAL — 4

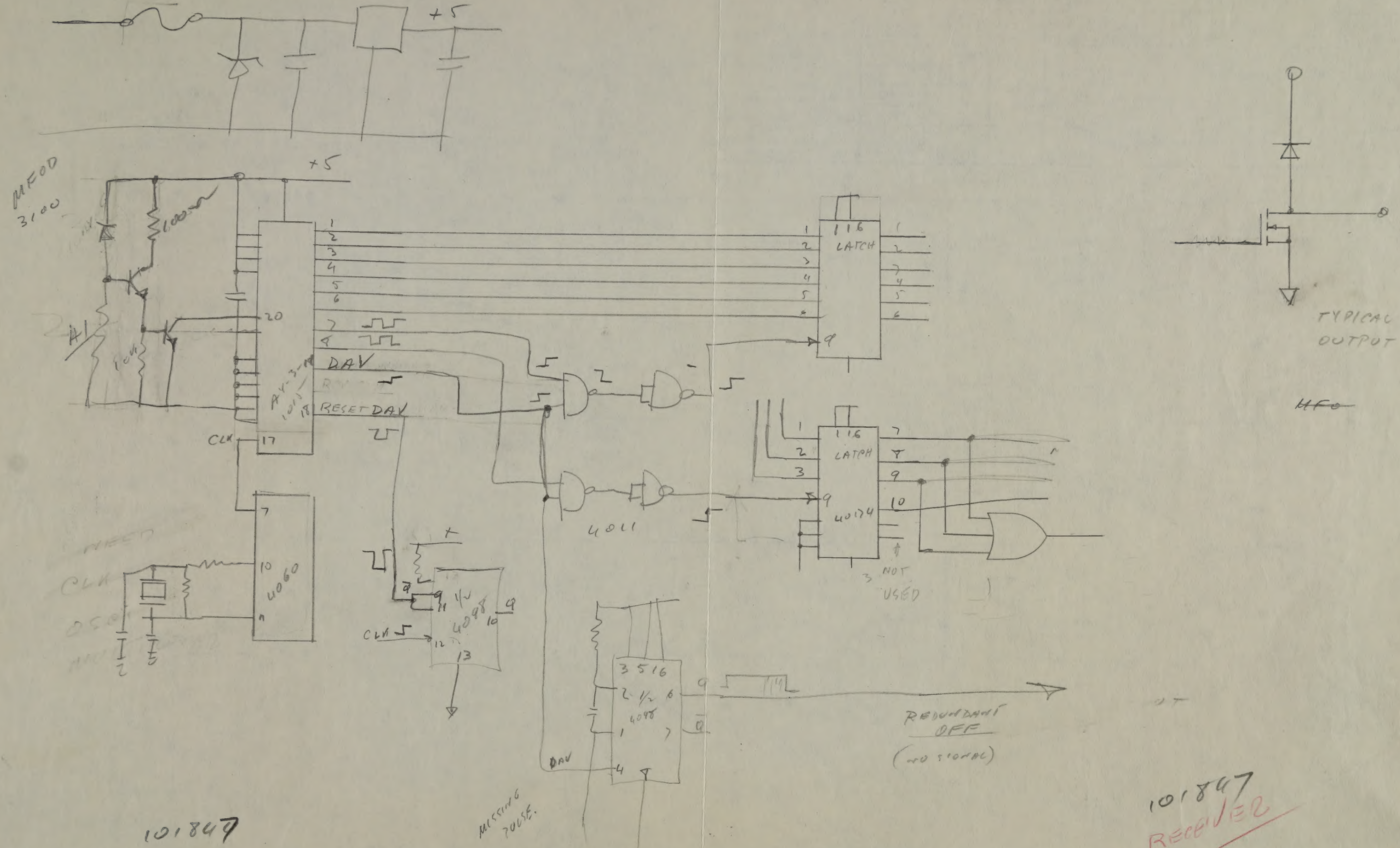
4.7K RES. NETWORK DIP — LOTS

905-145-5000 ~~[illegible]~~

AMPHENOL FIBER OPTICS RECEPTC. — 10

$\boxed{\text{NO CABLE}}$

2N4125, 2N4123, 4098 STOCK
P6KE22 - STOCK.
CAP. & RES. STOCK



101847

101847
RECEIVER

PARTS ON HAND

AY-3-1015D — 2

MC 3423 - O/V. — 5

74HC4060 - OSC/COUNT — 14

78L05 - REG. — 2

4082 - AND — 1 +

4503 - TRI-STATE BUFF — 12

40174 - LATCH — 2

15 N05L - MOSFETS — 30

MFOE-3200 EMITER — 4

MFOD-3100 DETECTOR — 4

ME-332-1033 XTAL — 9

27PF FOR XTAL — 4

4.7K RES. NETWORK DIP — LOTS

905-145-5000

AMPHENOL FIBER OPTICS RECEPTC. — 10

$\boxed{\text{NO CABLE}}$

2N4125, 2N4123, 4098 STOCK

P6KE22 - STOCK.

CAP. & RES. STOCK

104 = 1004
105 = 1M
106 = 10M